A CALCULATOR OPTION FOR THE TEKTRONIX 4010 COMPUTER GRAPHICS TERMINAL

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THESIS

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4010 COMPUTER GRAPHICS TERMINAL

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ABSTRACT

Recent advances in Metal-Oxide-Semiconductor/Large-Scale-Integration (MOS/LSI) circuits have made large amounts of computational capability available in small packages. One such MOS/LSI circuit, a business-format, four-function calculator, is utilized to provide a fixed-function form of intelligence in the Tektronix 4010 Computer Display Terminal. Discussion of important circuit design concepts from preliminary considerations to final testing and results is presented. Sample calculations and instructions for calculator operation are given as appendices.

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I. INTRODUCTION

Artificial intelligence has been present in many forms since man devised his first tool. However, a firm definition of this form of intelligence has never been agreed upon. Most researchers consider artificial intelligence as that intelligence which is neither animal nor man intelligence. If this is the case, then the question of whether a machine is intelligent or not depends entirely on the definition of intelligence.

A. MACHINE INTELLIGENCE

Machine intelligence, its sources, forms, and definition have been the topic of continual research for a number of years. Recent technological advances in electronics have resulted in computing machines that far exceed man in speed in certain tasks. But do these computers really possess intelligence? Reference [14] defines intelligent machines as those that are able to perform tasks that, until recently, only human beings could perform and, to perform them with effectiveness and speed comparable to a human. By this definition then, computers as well as many other machines could be considered to be intelligent. However, most researchers in the field of artificial intelligence list the ability to learn as a key element to intelligence. A computer can learn through programming to perform higher level tasks previously performed by man; but its decision making

processes could not, until recently, be changed except through reprogramming by man. Reference [15] states that intelligence is multipurpose and involves the ability to learn through experience. By these standards, present-day electronic computing machines that have fixed functions possess problem solving ability but do not possess intelligence. Only present research in adaptive programming and networks is tending towards true intelligence in machines.

B. INTELLIGENT COMPUTER TERMINALS

The first computer terminal devices were simply communications interfaces. Some device was needed to translate between the man and the machine. This was supplied by the computer terminal. With the invention of integrated circuits and the advances in technology made subsequent to that event, an ever-increasing amount of functional potential has been available in a smaller and smaller circuit size. This has resulted in a trend, in the field of computer devices, towards what is termed an "intelligent terminal". For the purposes of this paper, an intelligent terminal will be considered as one that possesses functional capability or computational ability beyond the basic code conversion process of the terminal device.

There are two implementations of terminal intelligence. The first of these and the more common is to provide a certain degree of software programming capability within the terminal itself. The terminal is then used for local data

processing, sorting, or formating which is unique to the terminal system, thus allowing the main computer to remain free for the more complex computational tasks. The second approach could be considered a hardware approach. Certain fixed computational functions or capabilities are built into the terminal and may be performed independent of the main computer.

Within the last few years, greatly increased density with good production yield in Metal-Oxide-Semiconductor (MOS) Technology has enabled manufacturers to place complete arithmetic calculators, and even complete microcomputers on just a few integrated circuits. This computational capability in a small package is ideally suited for the second approach to intelligent terminals, where processing speed is not a critical factor. The remainder of this thesis describes a design project to increase the intelligence level of a general purpose graphics terminal through use of a MOS/LSI calculator circuit.

II. PRELIMINARY CONSIDERATIONS AND DESIGN

A. INTRODUCTION

As an exercise in the application of present-day integrated circuits in the area of intelligent terminals, a design project was undertaken during an industrial tour period at the Information and Display Products (I.D.P.) division of Tektronix, Inc. The initial concept and preliminary design criteria for the project came from the marketing staff of I.D.P.

1. Project Concept

The initial concept was to design and produce as an option to the Tektronix 4010 terminal, a terminal auxiliary card, which, when inserted in the base of the terminal, would allow the operator to utilize the terminal as a business format, four function calculator. The calculator option was to utilize the storage feature of the 4010 CRT to record all calculations subsequent to the last screen erasure. This feature would allow a permanent record of calculations to be made through the use of a hard-copy unit. The calculator card was to be offered as an option to the basic terminal, thus making the terminal more attractive to large business-oriented customers.

2. Initial Design Criteria

The initial design criteria received were general in nature and are listed below.

a. Product Size

The entire calculator option should fit on the terminal auxiliary card normally used by Tektronix for interfacing of the 4010 terminal to the various types of computers and peripheral devices.

b. Capabilities

The calculator should have the four functions of addition, subtraction, multiplication, and division with at least eight digits in the resultant display.

c. Options

The operator should have the option of entering data and operations into the calculator, either from the normal terminal keyboard or from a special numerical calculator keyboard available on a cable extension from the calculator option card.

B. PRELIMINARY DESIGN CONSIDERATIONS

As a preliminary to the initial design of the calculator option, a study was made of the various operating conditions and possible major components or units to be used. A discussion of the results of that study, and a description of the various units and their respective performance criteria follows.

1. Tektronix 4010 Terminal

The Tektronix 4010 Computer Display Terminal is a communications link and display device for use with a wide range of computer systems. The terminal itself is very complex, therefore detail will be given only to those areas directly related to the design of the calculator interface. Complete terminal circuitry detail and operation is available in references [1, 2, 3]. The problems involved in interfacing any external device with the 4010 terminal are primarily ones of communication; what method of information transmission to use, and what timing conditions are necessary to get the information into the terminal and onto the screen. These areas, as well as several others, will be discussed in this section.

a. Buss Structure and Codes

The 4010 terminal uses a parallel buss structure for all internal data communication. This communication is comprised of data transfers between the several sections of the basic graphics terminal and data transfers between these sections and any external interfacing device. An example

of such an interface device isthe option 1 basic serial interface which permits communications between the 4010 terminal and a large number of present day computer systems through use of a MODEM.

The buss structure consists of 72 individual busses including power connections, clocking, synchronization signals, and data bits. Transistor-Transistor Logic (TTL) is utilized throughout the logic portion of the terminal; and the major portion of the buss structure operates on the usual TTL logic levels. In order to permit the multiple use of any given buss by the several units that may be connected to it, a low-active logic system is used. Each buss functioning as a logic communication link has its own individual pull-up resistor to +5 volts, and may be controlled by any number of open-collector buffer gates. The terminal relies entirely on proper timing and synchronization in order to ensure that the various terminal modules and interfacing devices do not interfere with each other. Connection to any given buss is made by edge connector of the particular card as it is inserted into the terminal base. Terminal auxiliary cards of the proper size and with edge connections to all 72 busses in the structure are available. One of these cards was used for the prototype of the calculator option. At this time, it was decided that the calculator option would be placed on a single terminal auxiliary card and would communicate with the 4010 terminal through the terminal buss structure in the same fashion as a larger

external computer. All necessary interfacing and control circuit would be contained on the same card.

The next problem directly encountered was the choice of codes to be used in the terminal/calculator communication. The 4010 terminal utilizes the American Standard Code for Information Interchange (ASCII). This code (figure 1) contains all of the alphabetical, numerical and control functions necessary for the alphanumerical (Alpha) mode of operation of the terminal; and is used through special procedures for the graphical (Graph) mode as well. For the calculator option, it was decided to use the Alpha mode of terminal operation since all the necessary numbers, decimal point, and symbols to represent operations were readily available. In addition the four bit row code of the ten numbers in ASCII is the same as the binary coded decimal (BCD) representation used internally by all calculators in present use. It was felt that proper choice of the remaining symbols and control codes could result in a minimization of the decoding and interfacing circuitry in the final design. The bits of the ASCII code are represented on the 4010 buss structure as $\overline{\text{BIT 1}}$ through $\overline{\text{BIT 8}}$ with $\overline{\text{BIT 8}}$ used as a party bit in certain operations.

c. Strobe and Timing Requirements

In addition to the proper selection of codes for data communication, consideration was given to the method and timing signals which must be used to get the data into, and to receive data from, the terminal circuitry.

BITS 7				0	0	0	0	1	1	1	1
			6	0	0	1	1	0	0	1	1
BITS			5	0	1	0	1	0	1	0	1
4	3	2	1	CONTROL		HIGH Y & X		LOW X		LOW Y	
0	0	0	0	NUL	DLE	SP	ø	@	P		p
0	0	0	1	SOH	DC1	!	1	A	Q	a	q
0	0	1	0	STX	DC2	"	2	B	R	b	r
0	0	1	1	ETX	DC3	#	3	C	S	c	s
0	1	0	0	EOT	DC4	$	4	D	T	d	t
0	1	0	1	ENQ	NAK	%	5	E	U	e	u
0	1	1	0	ACK	SYN	&	6	F	V	f	v
0	1	1	1	BEL	ETB	'	7	G	W	g	w
1	0	0	0	BS	CAN	(	8	H	X	h	x
1	0	0	1	HT	EM	)	9	I	Y	i	y
1	0	1	0	LF	SUB	*	:	J	Z	j	z
1	0	1	1	VT	ESC	+	;	K	[	k	{
1	1	0	0	FF	FS	,	<	L	\	l	|
1	1	0	1	CR	GS	-	=	M	]	m	}
1	1	1	0	SO	RS	.	>	N	^	n	~
1	1	1	1	ST	US	/	?	O	_	o	DEL

FIGURE 1 ASCII CODE CHART

Placing data on the ASCII bit busses is useless unless certain strobe and timing conditions accompany it. Reference [3] gives complete details to be considered in the design of a parallel interface for the 4010 terminal. The sequence of events necessary to enter an ASCII code into the terminal is shown in figure 2. Buss signals in addition to the data bits are $\overline{\text{CPUNT}}$ and $\overline{\text{TSTROBE}}$. $\overline{\text{CPUNT}}$ is a signal to all other interface units that use the buss structure that data is about to be placed on the buss structure by a given unit. $\overline{\text{TSTROBE}}$ provides a clocking of the data bits into latch storage on one of the basic terminal circuit boards. From this point on, processing of the data to the desired end of producing the symbol on the display screen is automatic. During the processing time the terminal generates another buss signal, $\overline{\text{TBUSY}}$, to indicate that it is busy. This signal provides an interrupt to all interface units.

For the reverse process of data transmission from the terminal to the computing device (by way of the interface unit), the buss $\overline{\text{CSTROBE}}$ is used. The terminal generates the data bits and generates $\overline{\text{CSTROBE}}$. This signal strobes the data into the interface unit where it is further processed and sent to the computer. An interrupt for this transmission is provided by $\overline{\text{CBUSY}}$, which indicates to the terminal that the computer is busy and cannot receive data at that moment.

It was decided to use this same communications timing and interrupt mechanism in the design of the

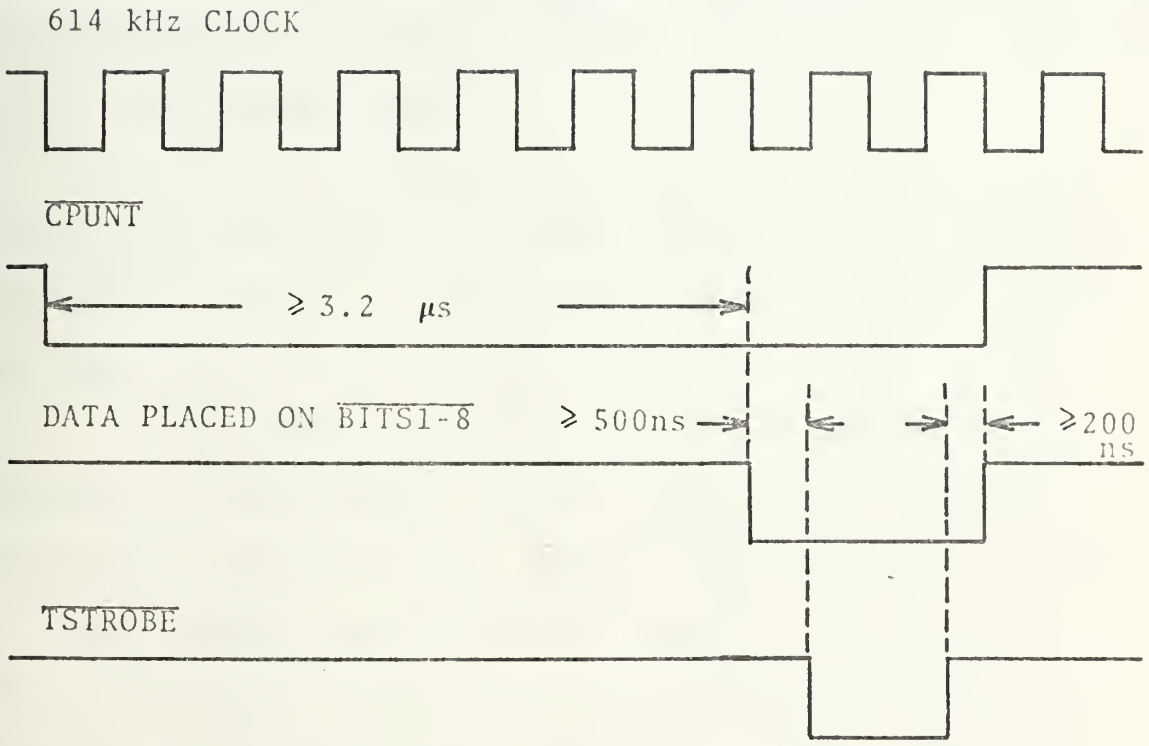


FIGURE 2 4010 TERMINAL TIMING CONSIDERATIONS

calculator option. The calculator would receive numerical inputs and operational commands from the terminal buss structure through use of $\overline{\text{BIT 1}}$ - $\overline{\text{BIT 8}}$ and $\overline{\text{CSTROBE}}$, and would generate $\overline{\text{CBUSY}}$ to indicate that it was busy with a given calculation. Upon completion of the calculation, the calculator would send the result in the proper format, and with necessary sign and error conditions to the terminal over the same data busses by use of $\overline{\text{TSTROBE}}$. Interrupt to this transmission would be provided by $\overline{\text{TBUSY}}$, generated by the terminal.

d. Screen Format

Since the display of calculator inputs, operations, and results was to be made through use of the terminal display screen, a study of the operation of this device was made.

The 4010 terminal uses a grid transfer type storage tube for display. Once a character or symbol is written onto the screen, it remains there until the screen is erased through use of the PAGE signal. In the Alpha mode, the terminal can display any character contained in the 6-bit TTY subset of the ASCII code. A non-storing cursor is displayed on the screen to indicate the next writing position. This is the alphanumeric or Alpha cursor. The display screen allows up to 35 lines of information with a maximum of 74 characters in each line. This screen format is shown in figure 3. There are left and right margins with an automatic carriage return and line feed at the right margin. When turned on, the 4010 will automatically reset

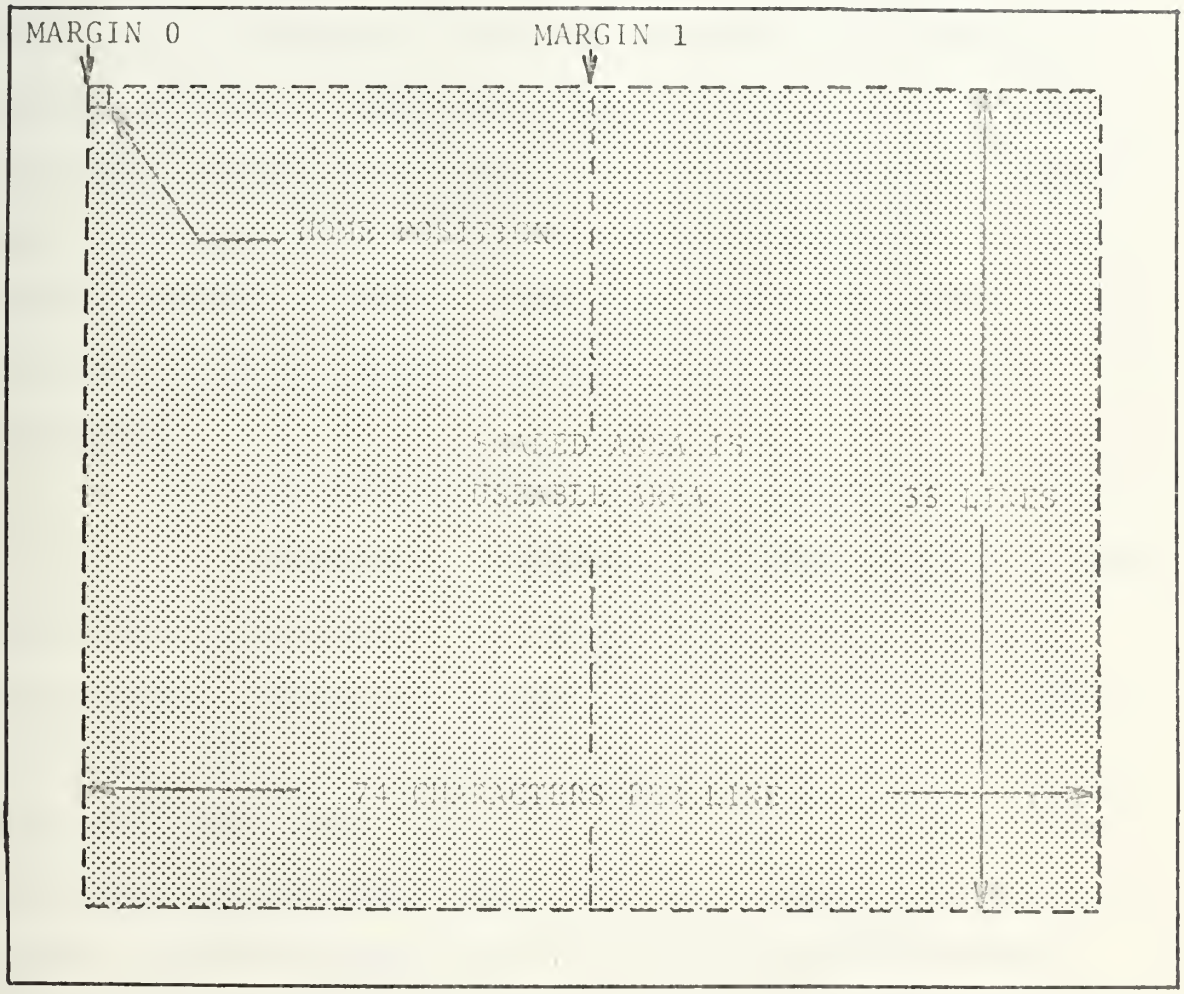


FIGURE 3 ALPHA MODE DISPLAY SCREEN FORMAT

to the Alpha mode with the cursor at the home position in the upper left hand corner at margin 0. This is the first line, first character position. In addition, if the actual line width is less than half the width of the screen, strobe movement to upper center of the screen at margin 1 is available as an option. This enables the use of the left half of the screen and then the right half for adjacent columns of text. Since the single line entries from the calculator option were expected to be less than 37 characters in length, it was decided to use this feature in the intiial design to maximize the number of calculations that could be displayed before erasure of the screen became necessary.

e. Power Availability

In addition, availability of the voltages necessary for the calculator was considered. Since the only calculators available use Metal-Oxide-Semiconductor (MOS) circuitry, the necessary bias voltages must be present. Reference [8] shows that the highest bias potential necessary for high-threshold MOS circuits is approximately 27 volts. This is within the 30 volt potential difference provided by the +15 volt and -15 volt buss within the terminal. In addition sufficient current is available at these busses to supply the low requirements of the MOS circuitry.

2. Screen Format Considerations

Electronic calculators are available with two modes of operation. The algebraic version operates in a manner

such as that used in the usual algebraic equation; a series of numbers and operations ending with an equal sign and then the result. The business (or adding machine) format has been derived for the normal sequence of bookkeeping used by accountants. A numerical entry is made followed by an operator which indicates whether the entry is to be added or subtracted from the previous balance. Since the original concept of the 4010 calculator option was that it provide a means of business calculation, the business format calculator was considered to be best suited. Consideration was next given to the screen format that would give the clearest representation of calculations and results.

a. Basic Screen Format

The following items were considered necessary to indicate to the calculator operator, proper sequencing and results.

(1) Input Numbers and Decimal. As each number is entered, it should print on the screen so that the operator can verify the entry. The decimal point position in the input is similarly verified. This portion of the input would be, by necessity, in floating point form.

(2) Operation Commands. A symbol indicating the operation to be performed is printed to verify and record the operation, and to terminate the entry sequence.

(3) Error and Sign Conditions. Upon completion of the calculation, sign and error conditions would be indicated. Error of any sort would be indicated both

visually by symbol on the screen, and audibly by sounding the terminal "bell". The sign of the result would be indicated to give a true credit-balance type display. The sign and error indications as well as the result to follow would be in vertical alignment with the codes of previous lines to present a well-ordered display.

(4) Result. The result and decimal point would be printed in an aligned balance column immediately following indication of sign.

b. Automatic Margining

The automatic margining feature described in reference [1] was considered desirable to permit fullest use of the screen area. In addition, a carriage return and line feed would be generated at the end of each line sequence in order to provide a return to either margin 0 or margin 1.

3. Calculator Considerations

The choice of which calculator to use was the most important preliminary consideration made. Choice of the right calculator could result in a minimum of interfacing and thus a reduction in manufacturing cost, while an improper choice of calculator could lead to eventual project failure. Some of the features considered are discussed in the following paragraphs.

a. Mode of Operation

All of the basic MOS calculators considered have the four operations: addition, subtraction, multiplication, and division. As discussed in the previous section on

screen format, the business mode of operation was selected for ease of presenting data and results to the terminal in a business, bookkeeping fashion. The only other prime consideration in operation was the method of point placement. It was felt that a calculator with both floating point and fixed point modes of operation would satisfy the needs of the dollars and cents balance column, and provide the accuracy of a floating point machine if needed.

b. Constant Feature

Some calculators offer a constant feature which allows repeated multiplications or divisions of a series of numbers by a single constant without re-entry of the constant for every operation. This feature was considered desirable in the business format calculator for example, to calculate the tax as a fixed percentage of a long series of individual numbers. In this case each number and its percentage would appear opposite each other on the same line for ease of later referral.

c. Automatic Round-Off

Automatic round-off would be used in conjunction with the fixed-point mode of operation, and the multiplication and division operations to prove a 5/4 round-off in the result. This would provide a result correct to the nearest cent for any financial calculation involving multiplication or division.

d. Output Structure

The output structure of most electronic calculators are of two forms. The more usual form provides

numerical information decoded to conform to a 7-segment numerical display, and digit information in the form of individual digit drive lines. The second, and less usual, form presents numerical data in BCD form and digit information in either the above form or in binary form. Both forms are designed to permit a time-multiplexed display where the numerical data present at any given time on the data lines corresponds to the digit line active at that given time. The coded form of output structure was preferred since it permitted direct interface of the output data lines of the calculator with the terminal circuitry utilizing the ASCII code.

e. Interfacing

Recent advances in the ion-implantation type production of MOS integrated circuits have enabled manufacturers to reduce the threshold voltage of the MOS circuitry. This not only results in a more efficient circuit but allows ease of interfacing of these devices with TTL logic levels. Therefore, a low-threshold MOS calculator utilizing a logic scheme compatible with TTL logic was considered as the most desirable.

f. Size

Basic four-function calculators of the type discussed above are available in sizes from six-chip sets down to single chip calculators. For reasons of power, economy, and size limitations, only single chip calculators were considered for the project.

The comparative study of all available calculators with respect to the points discussed is beyond the scope of this thesis. The final choice was to utilzie the Texas Instruments TMS-0100 NC one-chip calculator series and more specifically the TMS-0102 NC version. Complete operational properties and electrical specifications for this series are given in reference [12]. Although the output structure of the particular calculator chosen was not of the desired type, all of the good features discussed in the other sections were present in this calculator. In addition, the calculator provided the eight digits required by the initial design criteria.

4. Preliminary Design

As a preliminary to final design of the circuits, choice of codes was finalized to correspond to the calculator circuit chosen, a sequence of events or operation was determined and a switching structure appropriate to generate this sequence was selected.

a. Code Selection

A minimal set of codes necessary for complete operation was selected by first separating the codes into two sub-sets. Table 1 shows the codes necessary for communication from the terminal to the calculator, the ASCII symbols chosen, and a description of the operation performed. These particular selections permit a complete description of the operation by the first four bits of the ASCII code with one ambiguity. The exception is the code 1100 which could

TABLE 1 CALCULATOR OPTION INPUT CODES

KEYBOARD SUMBOL	OPERATION	ASCII
0	ENTER 0	Ø
1	ENTER 1	1
2	ENTER 2	2
3	ENTER 3	3
4	ENTER 4	4
5	ENTER 5	5
6	ENTER 6	6
7	ENTER 7	7
8	ENTER 8	8
9	ENTER 9	9
+=	ADDITION	+
-=	SUBTRACTION	-
X	MULTIPLICATION	*
÷	DIVISION	/
C	CLEAR ALL REGISTERS	FF
CE	CLEAR ENTRY REGISTER	FS
.	ENTER DECIMAL	.

represent either a C or CE operation. Bit 5 is necessary here to distinguish between the two operations. All operations except C and CE result in a printed symbol on the terminal display screen. The codes chosen for C and CE are, at present, non-printing.

Codes necessary for data and control function transmission between the calculator option and the 4010 terminal are shown in table 2. Some of the codes are common with the input code set, but used in a slightly different manner. Others such as BEL, NUL, CR, #, and LF are unique to the output set to control the functioning of the terminal. The first six bits of the ASCII code completely describe the set of output codes. All output codes result in terminal action, but the control codes and SP do not result in a display symbol.

b. Single Line Sequence

The choice of codes combined with the number of digits in the calculator result allowed selection of a sequence of events for a single line. This sequence is described in figure 4. There are 36 character spaces available between margin 0 and margin 1 on the screen. Starting at margin 0 is a field, variable from one to ten spaces, consisting of input numbers, one decimal point, and one operand. At the end of the input sequence, additional spaces are added as necessary to make up a total of sixteen. This correctly positions the remainder of the line in the same position for every line. At this point error conditions

TABLE 2 CALCULATOR OPTION OUTPUT CODES

OUTPUT FUNCTION	OPERATION	ASCII
0	XMIT 0	0
1	XMIT 1	1
2	XMIT 2	2
3	XMIT 3	3
4	XMIT 4	4
5	XMIT 5	5
6	XMIT 6	6
7	XMIT 7	7
8	XMIT 8	8
9	XMIT 9	9
.	XMIT DECIMAL POINT	.
SIGN OF RESULT	XMIT SPACE OR MINUS SIGN	SP or -
ERROR CONDITIONS	XMIT BELL, OR NULL	BEL, NUL
ERROR CONDITIONS	XMIT # OR SPACE	# or SP
LEADING ZERO	XMIT SPACE	SP
CARRIAGE RETURN	XMIT CARRIAGE RETURN	CR
LINE FEED	XMIT LINE FEED	LF

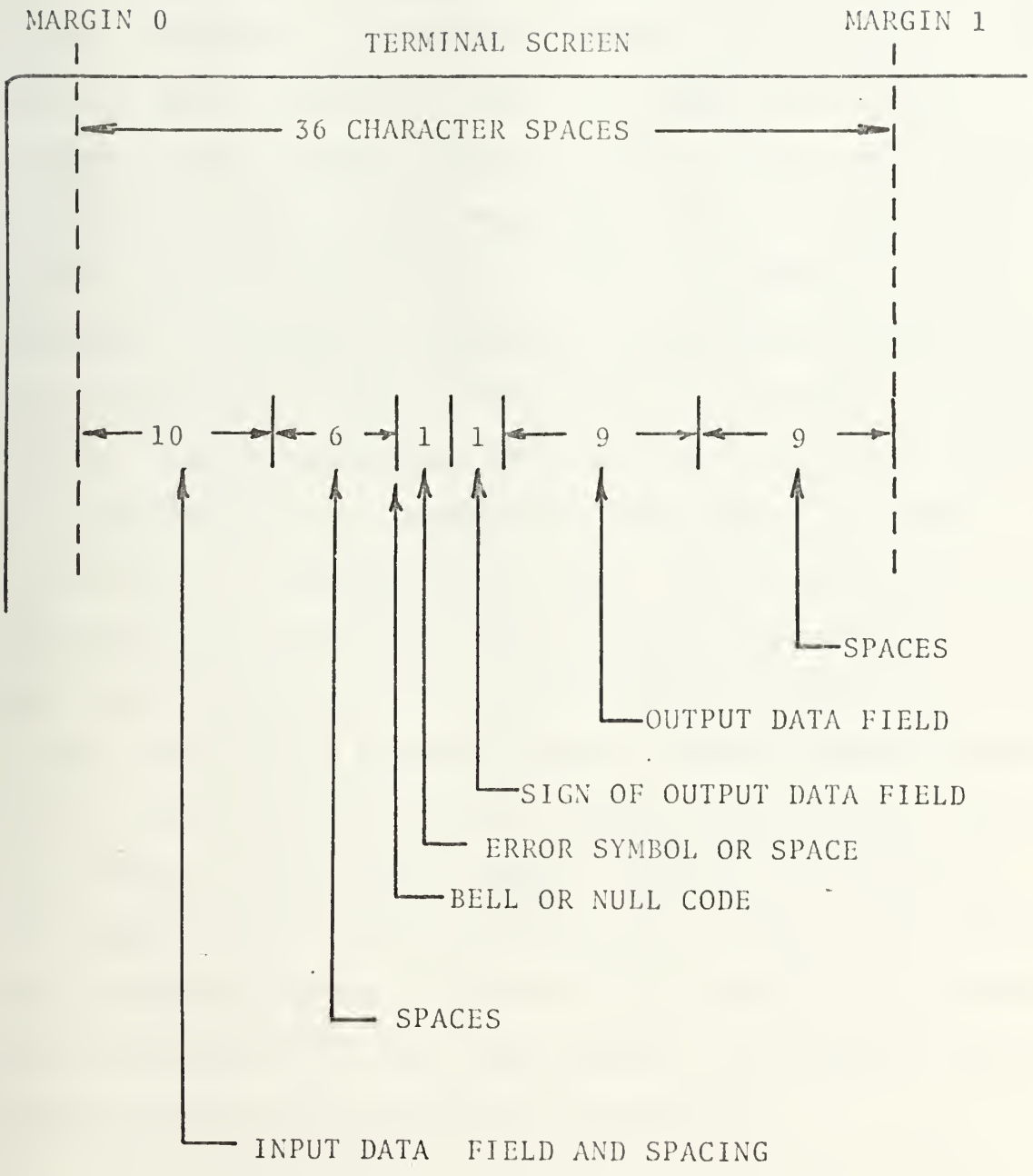


FIGURE 4 SINGLE LINE SEQUENCE

are indicated. First the terminal bell is sounded if an error condition is present. If not, a null code is transmitted. Neither of these codes results in a character space. Next if error conditions exist, a # symbol is sent and appears on the terminal display screen. If no error conditions exist, a space is transmitted. Both of these codes result in one character space. This concludes the error sequence. For the next character space, sign is displayed by transmitting a minus if the result is negative or a space if the result is positive. Finally the calculation result is transmitted, most significant digit first, with the decimal point correctly positioned. This is followed by a carriage return and line feed to position the cursor for the next line sequence. The overall sequence is shown in table 3 and consists of 8 separate phases. Twenty-seven character spaces are used which leaves a 9 character spacing between the margin 0 calculations and the margin 1 calculations. The input portion of the line sequence is controlled manually by keyboard input. Closure of an operation key shifts the line sequence to the output portion where control and return to the margin position is automatic.

c. Flow Chart

A flow chart representing the line sequence described above is shown in figure 5. The idle position is at key closure in phase 1. All phases that result in a single character space or no character space in the line sequence are simply straight-through paths or contain only

TABLE 3 SINGLE LINE SEQUENCE

PHASE	DESCRIPTION	DATA TRANSMITTED
1	DATA INPUT	KEYBOARD
2	SPACING	SPACES
3	ERROR 1	BELL or NULL
4	ERROR 2	# or SPACE
5	SIGN OF RESULT	- or SPACE
6	DATA OUTPUT	CALCULATOR DATA
7	CARRIAGE RETURN	CR
8	LINE FEED	LF

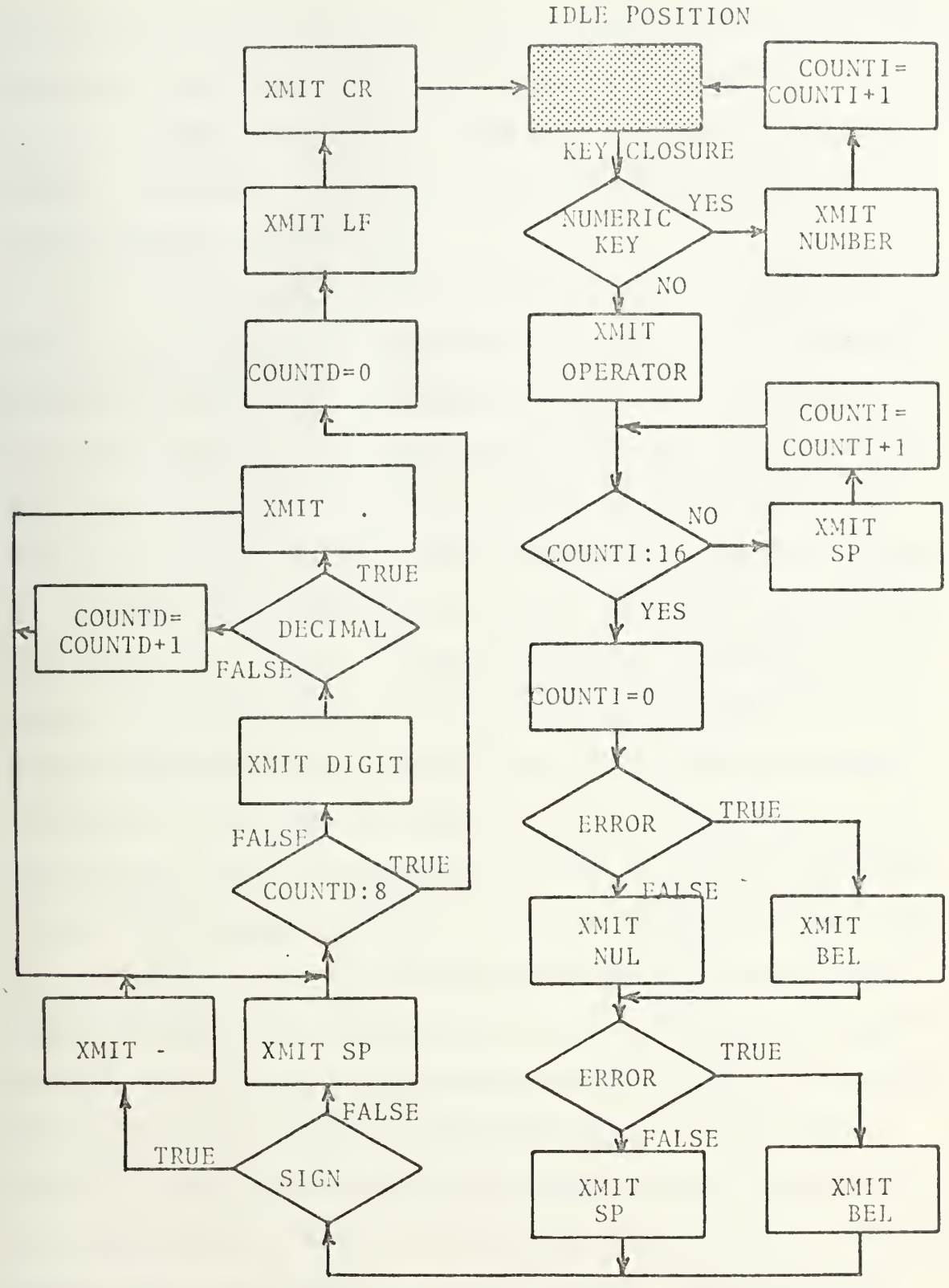


FIGURE 5 CALCULATOR OPTION FLOW CHART

conditional branching paths. Those phases related to multiple character spaces each contain an incremental count and comparison. These counters were initially termed COUNT I and COUNT D to represent the input counter and the digit counter respectively.

A typical sequence of events is as follows. Starting in phase 1, a key closure is made. The closure is tested to see if it is an operation key. If not, COUNT I is incremented by 1 and the sequencer returns to the idle position to wait for the next input. If the closure is found to be an operation, the calculator sequences to phase 2. In phase two COUNT I is tested to see if it has reached the count 16. If not, a single space is transmitted, the counter incremented by 1, and then retested. When the count reaches 16, the counter resets and action sequences to phase 3. In phase 3, error conditions are tested and if found true, BEL is transmitted. Phase 4 is the second error phase. Here again, the test is on the same error conditions as in phase 3, only with different transmissions as shown. Phase 5 results in transmission of a minus sign for negative results and a space for positive results. Phase 6 transmits the calculation result to the terminal in correct form. Since the TMS-0102 NC calculator utilizes an 8 digit result, the comparison of COUNT D is with its eighth count. Initially COUNT D will be reset or in the 0 state. The digits are transmitted sequentially starting with the most significant digit. Therefore, the presence of the decimal point in any

given digit time frame interrupts the digit sequence and allows transmission of a decimal point following that digit and prior to transmission of the next digit. Completion of 8 digit transmissions results in an exit to phases 7 and 8 and a return to the idle position. This type of decimal interrupt is necessary since in the calculator, the decimal occupies the same time frame or character space. Since the TMS-0102 NC uses a right-hand point display system, transmission of the decimal point must follow the digit contained in the same calculator digit time frame.

d. Special Structure Block Diagram

With the finalization of the calculator option mode sequence and flow chart, some thought was given to the type of circuitry needed to generate this sequence of events. Any digital system can be implemented in a variety of ways. However, the primary consideration in this case, was to keep the cost as low as possible. The required special purpose structure can be described in terms of the general form as presented in chapter 6 of reference [4], and as shown in figure 6. The two major parts of this structure are:

(1) The Data Processing Circuitry.

(2) The Timing and Mode Circuitry.

The data processing circuitry includes input devices such as multiplexers, analog-to-digital converters, switches and keyboards. It also includes output devices such as stepping motors, digital-to-analog converters, and display of various types. It includes any data storage

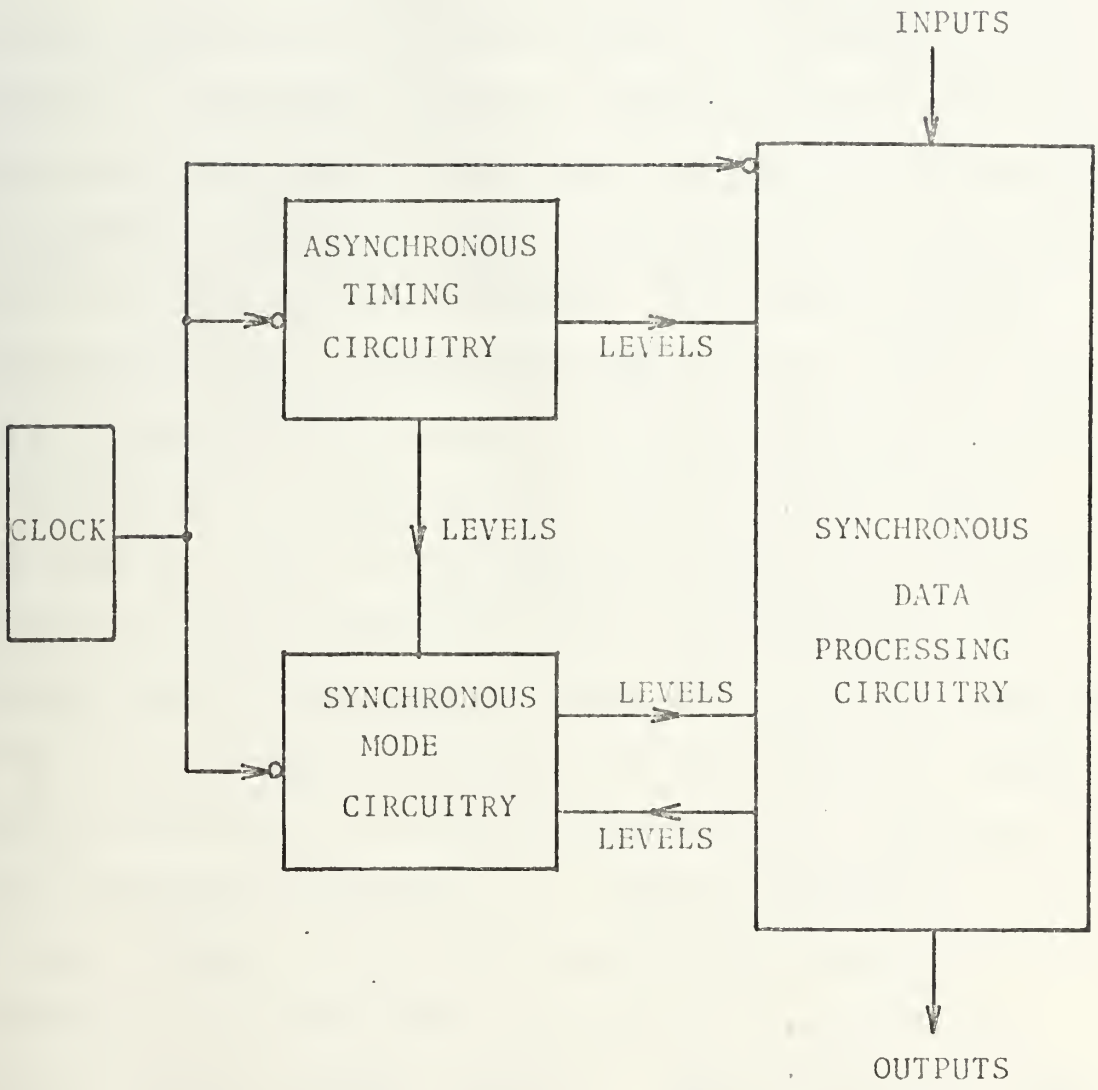


FIGURE 6 GENERAL FORM OF SPECIAL PURPOSE STRUCTURE

necessary to the problem. Finally, it includes whatever structures are appropriate for implementing the algorithms that take the system inputs and generate the system outputs.

The timing and mode circuitry basically serves the same function as the program does in a general-purpose computer. The timing circuitry sequences those operations which are a function of time only. An example of this would be implementation of an algorithm where certain operations have to be done one after another. The timing circuitry might simply be an asynchronous binary counter which is in state 0 when operation begins. The data processing circuitry is controlled by levels coming from this binary counter, so that when the first clock transition occurs, the circuitry responds to those conditions which are enabled when the binary counter is in state 0. When the next clock transition occurs, the circuitry responds to those conditions enabled when the counter is in state 1, and so forth. The mode circuitry sequences operations as a function of data as well as time. Inputs to the mode circuitry are functions of variables in the data processing circuitry and of time, derived from the timing circuitry. The mode circuitry generates circuit outputs which the data processing circuitry uses to sequence its operations. It also goes from state to state during clock transitions.

With the general form of the special purpose structure in mind, a block diagram of the calculator option was formed. This diagram is shown in figure 7. The phase

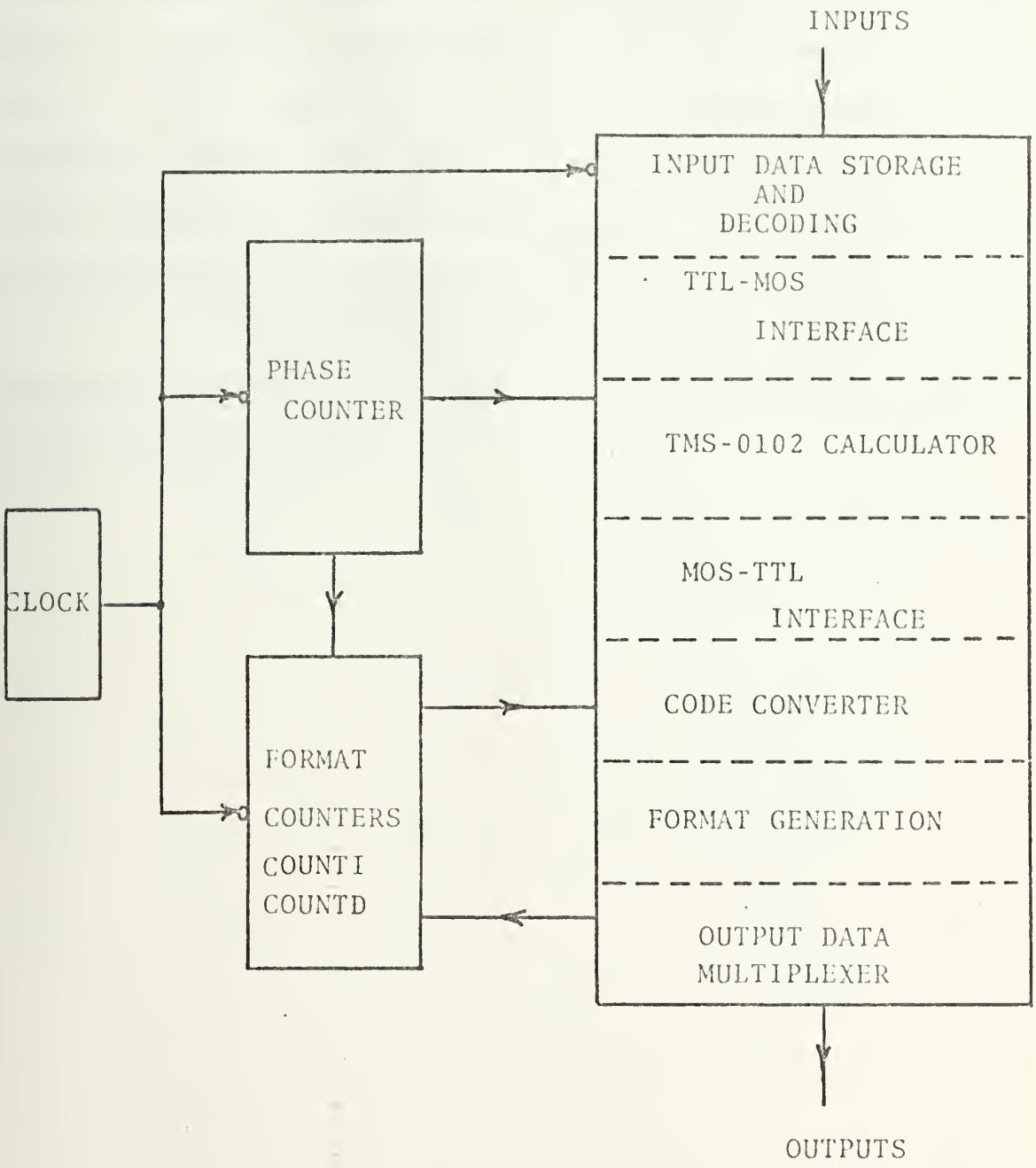


FIGURE 7 GENERAL BLOCK DIAGRAM OF THE 4010 CALCULATOR OPTION

counter provides asynchronously timed control levels to the other two sections. Format modes that are a function of the data as well as times are controlled by format counters COUNTI and COUNTD. The data processing section contains both the input and output data sections, the calculator and interfaces and other necessary format generation circuitry.

A final detailed design was next accomplished. Individual circuit details and operations will be discussed in the following section.

III. DETAILED CIRCUITS DESCRIPTION AND OPERATION

With the preliminary design completed, detailed design of the various sections proceeded. The results of that design will be discussed in this section in the form of a detailed circuit description and operational sequence for each of the sections or blocks. A block diagram of the final version of the 4010 calculator option is shown in figure 8. The final configuration of the calculator option closely resembles the special-purpose structure discussed in section II. Data and operational commands are received from the terminal buss structure through the input section and the correctly formated result is transmitted back through the same buss structure. In addition, a separate calculator keyboard is provided to permit rapid numerical and operational inputs to the system. Control circuits will be covered first in order to provide a better understanding of the data processing units when they are covered.

A. PHASE AND ENABLE CONTROL CIRCUITS

The phase and enable control circuits provide operational-level control to several of the other units. An understanding of the circuits and their function is necessary for the discussion to follow.

1. Enable Circuit

The enable circuit shown in figure 9 allows enabling and disabling of the calculator option without complete

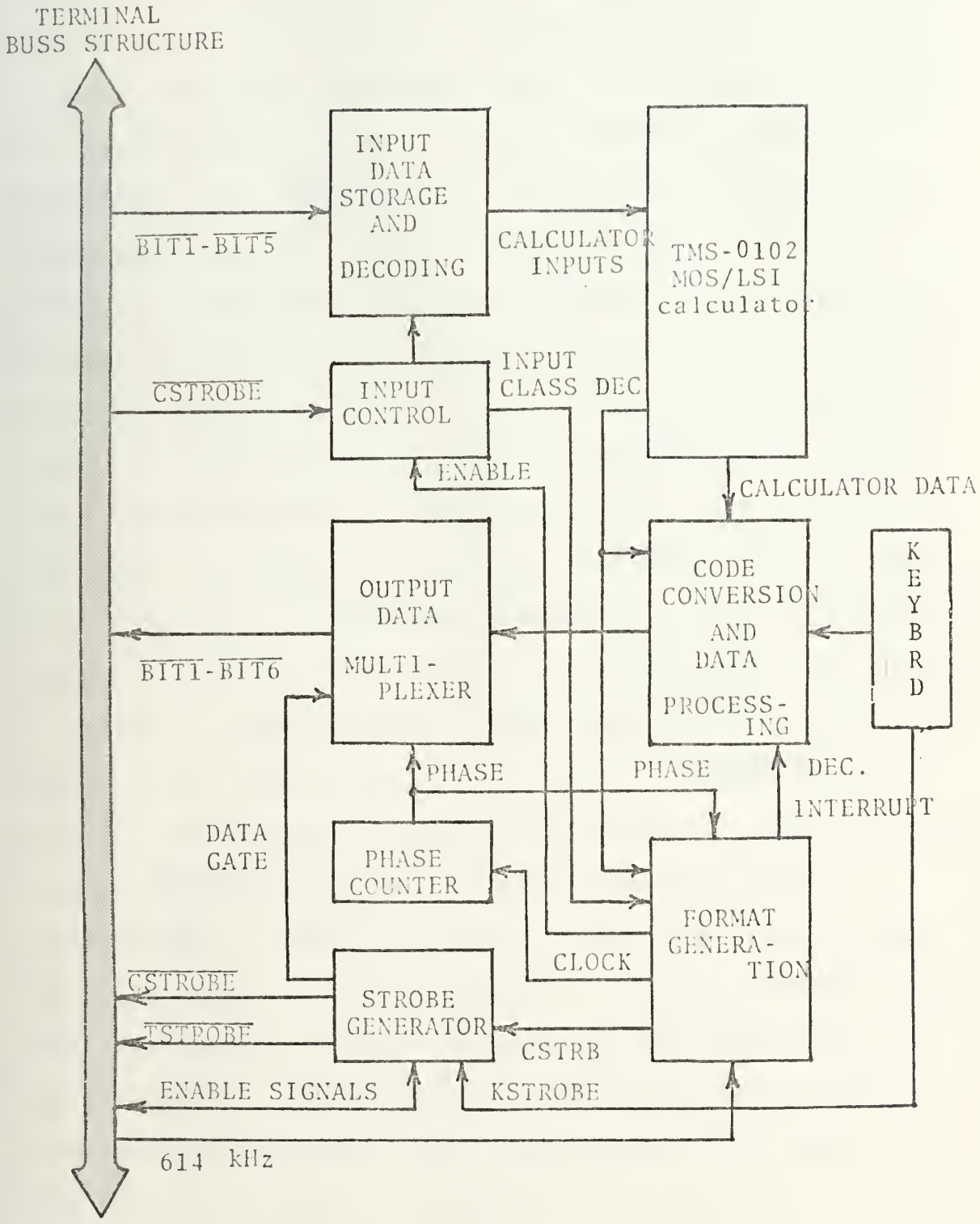


FIGURE 8 CALCULATOR OPTION BLOCK DIAGRAM

removal of the calculator circuit board from the terminal. The Tektronix 4010 terminal provides two general purpose rocker switches and indicator lamps on its keyboard. These are represented by the buss signals $\overline{\text{SWITCH 1}}$, $\overline{\text{SWITCH 2}}$, $\overline{\text{INDICATOR 1}}$, and $\overline{\text{INDICATOR 2}}$. In addition, a third rocker switch provides the ON-LINE / LOCAL function, and is represented on the buss structure by $\overline{\text{LOCAL}}$. Since the majority of all other interface devices are enabled by ON-LINE and disabled by LOCAL, it was decided to utilize the calculator while the terminal was in the LOCAL mode. This would eliminate mutual interference between the calculator option and any computer interfaces that might be installed in the terminal. In addition, $\overline{\text{SWITCH 1}}$ is used to provide a calculator ON/OFF option while in the LOCAL mode. As shown by figure 9, a combination of $\overline{\text{LOCAL}}$ and $\overline{\text{SWITCH 1}}$ provide the ENABLE level. This signal is fed back to $\overline{\text{INDICATOR 2}}$ to provide a front-panel, visual verification of "calculator on". Further, $\overline{\text{SWITCH 2}}$ is used in combination with ENABLE to provide $\overline{\text{KLOCK}}$. $\overline{\text{KLOCK}}$ is used to disable the terminal keyboard when the calculator keyboard is in use. $\overline{\text{SWITCH 2}}$ provides the option of choice of keyboard for data entry to the calculator. ENABLE also is fed to the strobe generation circuits to ensure that strobe outputs are generated only when the circuit is enabled.

2. Phase Control Circuit

The phase control circuit, shown in figure 10, is simply a 3 bit binary counter. A clocking input to the

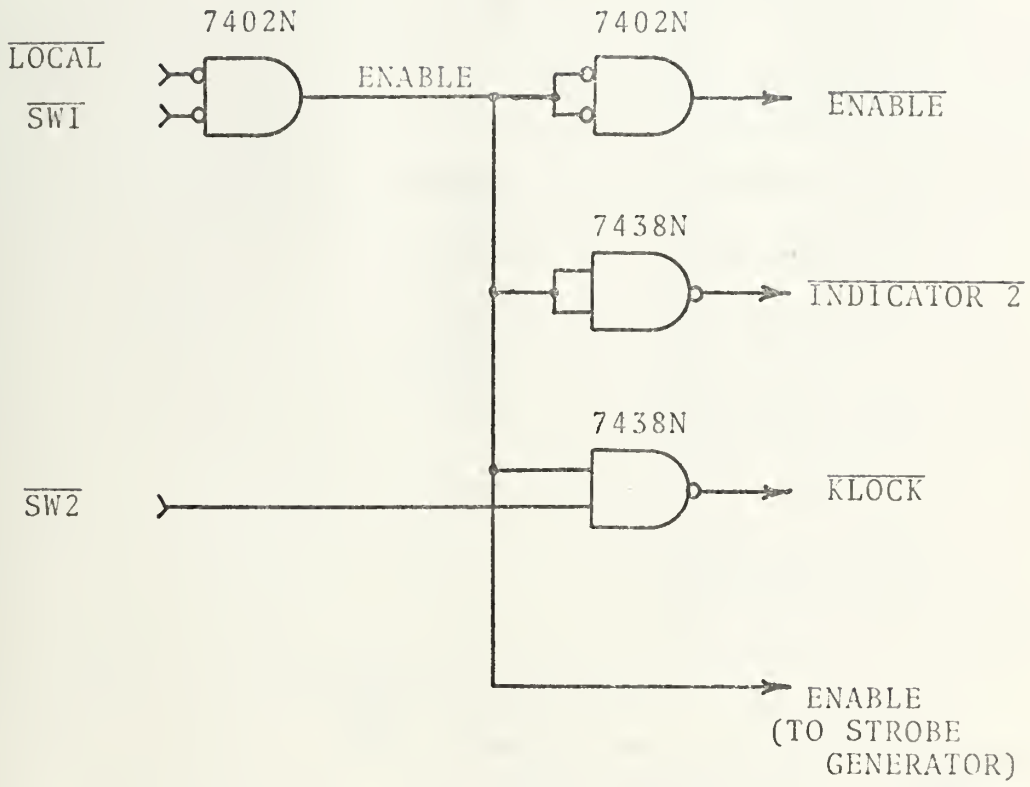


FIGURE 9 CALCULATOR OPTION ENABLE CIRCUIT

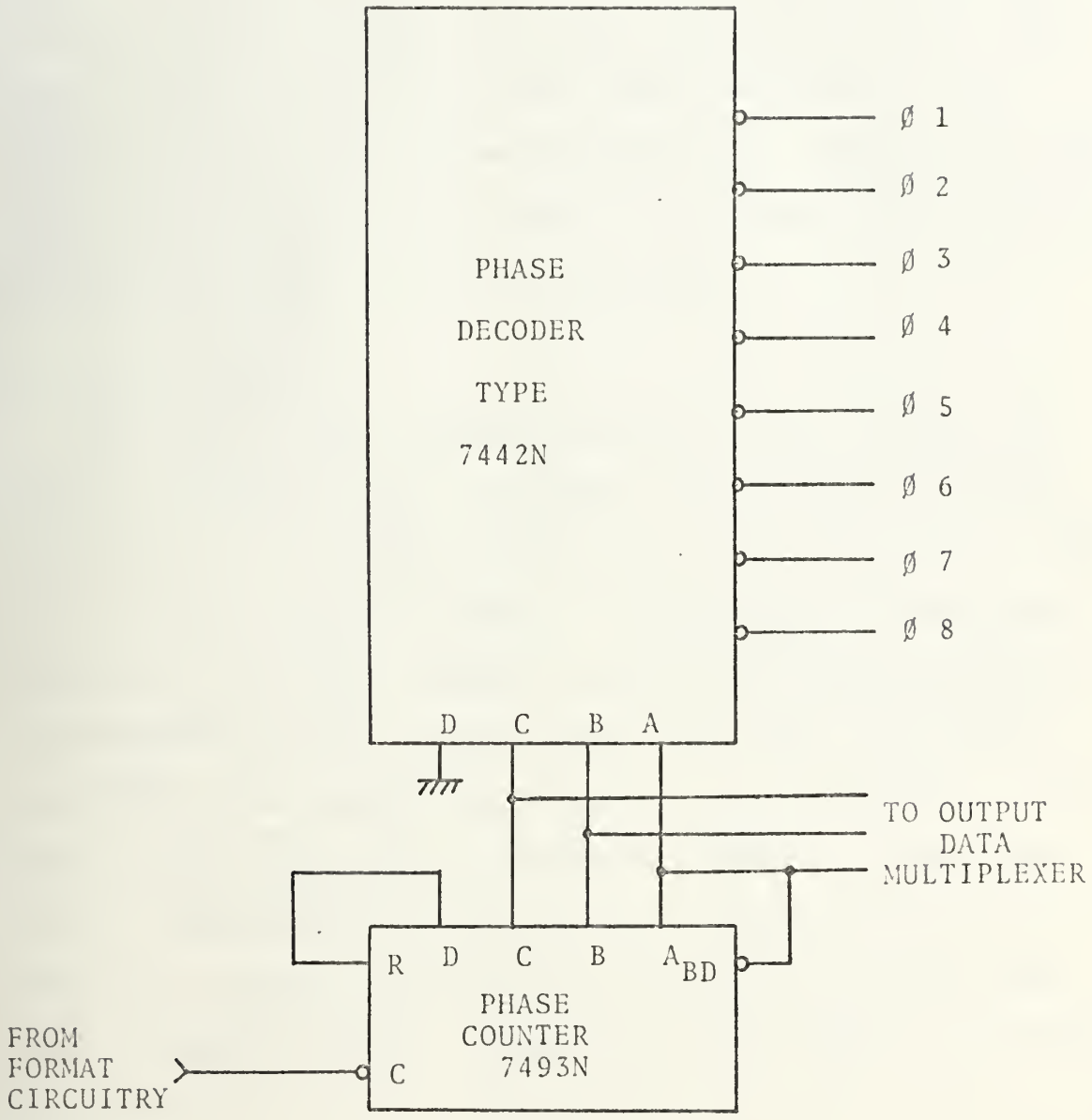


FIGURE 10 PHASE CONTROL CIRCUITRY

counter is received from the format circuitry at the completion of each phase and clocks the counter to the next phase. The counter outputs phase information in 3 bit binary form to the phase decoder and the output data multiplexer. The phase decoder decodes the binary phase information into individual, low-active phase control lines. These phase control lines are used by both input control and format control to effect necessary circuit sequencing.

B. INPUT SECTION

The input section contains temporary data storage, decoding of numerical and operational inputs, and the necessary control and timing functions to effect their entry into the calculator input interface. In order to perform these operations, the input section receives $\overline{\text{BIT 1}}$ through $\overline{\text{BIT 5}}$ and $\overline{\text{CSTROBE}}$ from the terminal buss structure, and $\overline{\text{Phase 1}}$ and $\overline{\text{ENABLE}}$ from the phase and enable control sections. The input section generates an artificial $\overline{\text{CBUSY}}$ for interrupt control and input type classification signals for use by the format section. The input section can be broken down into two general groups. Complete circuit details are shown in figure 11.

1. Temporary Data Storage and Decoding

The temporary storage and decoding group contains the data timing latches, decoder, and enable circuitry necessary to control entry of the data bits into the calculator. The primary design consideration is one of timing. The electrical specifications for the TMS-0100 NC series,

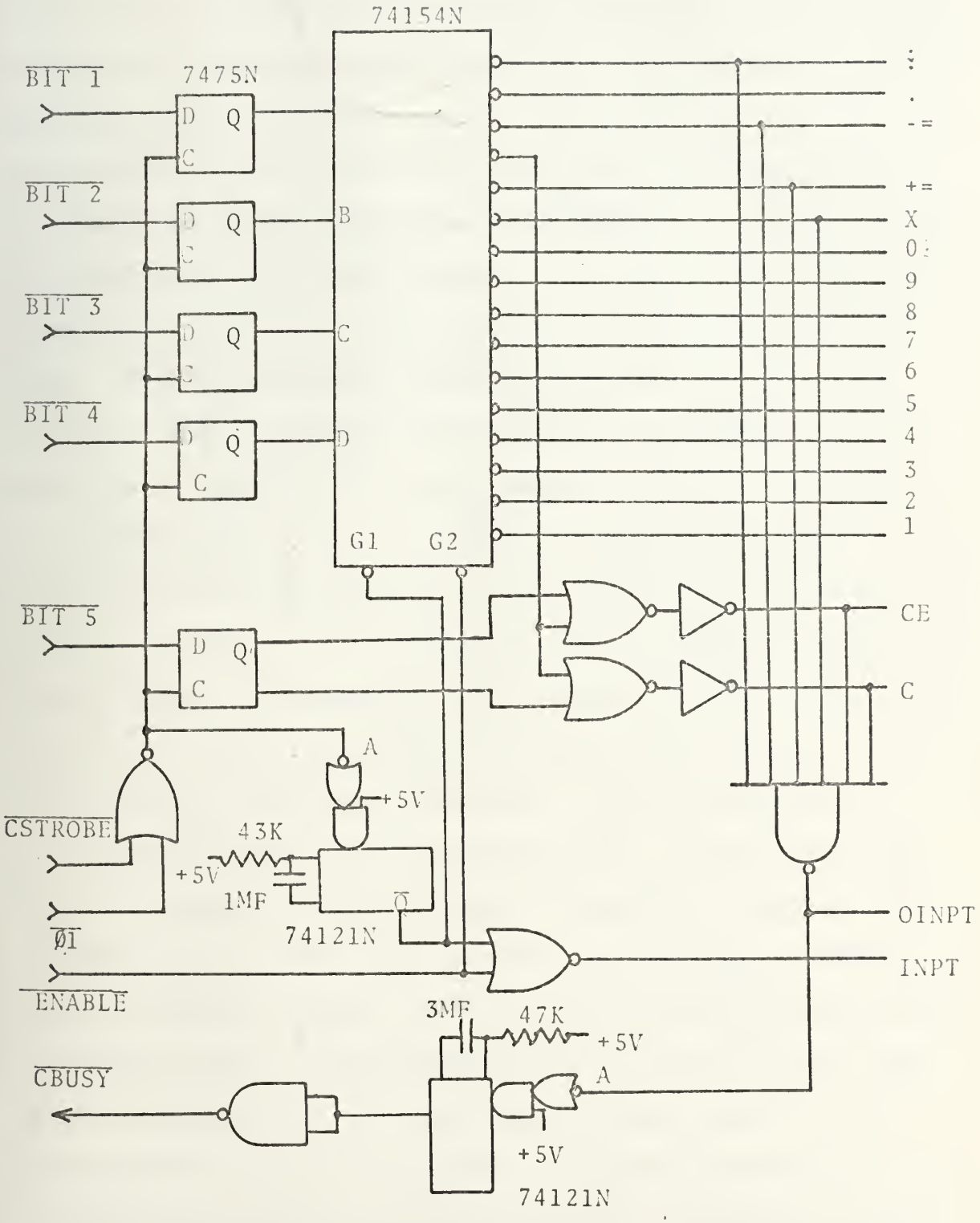


FIGURE 11 INPUT DATA STORAGE AND PROCESSING

reference [12] requires that any valid keyboard or data entry into the calculator be greater than 6000 clock periods in length. For a nominal calculator clock frequency of 307 kHz this means that for an entry to be considered valid, it must exist on the calculator input lines for greater than 19.5 ms. Since the data bits and $\overline{\text{CSTROBE}}$ are present on the terminal lines for only several s at most, a direct interface is not possible. Instead, the following procedure is used. The data bits are temporarily stored in five data latches. This is done by the presence of $\overline{\text{CSTROBE}}$ and the presence of phase 1, the input phase. That is, data will be latched into the input circuits only during phase 1 of the overall circuit sequence. The first four data bits are used as the four address lines of a type 74154N 4 line-to-16 line decoder. The decoder, when enabled, decodes these four bits into a single numerical or operational line, with the one ambiguity previously discussed. This ambiguity is reconciled by $\overline{\text{BIT 5}}$, the fifth data bit. Enabling of the decoder is done through terminals G1 and G2. Both must be at logical 0 to enable the decoder. G2 is simply $\overline{\text{ENABLE}}$ from the enable circuit. Thus no entries can be made to the calculator when the calculator option is not enabled. The second enable, G1, is derived from the data latch strobe. The negative edge of this strobe triggers a monostable multivibrator which is timed by external components to produce a pulse width of approximately 30 ms. This action produces a synthetic "key closure" greater than the required

minimum of 6000 clock cycles or 19.5 ms. The net effect is to produce, for each data input to the circuit, a single signal on one of the output lines corresponding to the input code. This signal is low-active and is of sufficient length to produce a valid entry to the calculator circuitry.

2. Control Signal Generation

There are three control signals generated in the input section. Two of these, INPT and OINPT, are simply input classifications and are used by the format section. INPT is generated whenever the calculator is enabled and there is an input of any kind. OINPT indicates that a given input is an operator. The decimal point is considered a numerical input, and is not included in the operational input set.

Since an indication of "calculator busy" is not available in any form from the TMS-0102 NC calculator, this signal must also be generated. This is done only for operational inputs by utilizing the negative edge of OINPT to trigger a second monostable multivibrator. Timing for this multivibrator is again derived from reference [12]. The worst case for computational time is the divide operation, which requires a maximum of 30000 clock cycles. Again for a clock frequency of 307 kHz, this means that $\overline{\text{CBUSY}}$ must be generated for approximately 95.3 ms in order to ensure that the buss signal overlaps actual calculation time. External timing components were selected to give an active time of around 100 ms for any given operational input. This signal

drives $\overline{\text{CBUSY}}$ through the usual 7438N open-collector buffer. The overall operational sequence of the input section is shown in figure 12.

C. CALCULATOR AND INTERFACING

In order to enter information into the calculator at the output lines, interfaces must be provided to permit this interchange of information between the two logic schemes. Further, the necessary clocking signals and bias voltages must be supplied to the calculator circuit.

1. Input Interface

The usual form of input is through a keyswitch matrix of the form shown in figure 13. The digit drive lines D1-D11 are the same digit lines used at the output to generate the time multiplexed display. Each is strobed sequentially in turn using a positive logic scheme. The two most important input lines are the keyboard numeric (KN) and the keyboard operation (KO) lines. If, for example, a strobe is obtained on input line KO during digit time frame D3, it would indicate the division operation.

This scheme of matrix input must be simulated using the input lines available at the output of the input section discussed in the previous section. At the same time the TTL logic levels must be shifted to conform to the MOS logic levels at the input. Reference [12] gives these logic levels as Vgg > logical 0 > Vss-6V, and Vss-1.5V > logical 1 > Vss. Interface at the input is not a difficult problem since the high input impedance of the input lines results in minimal

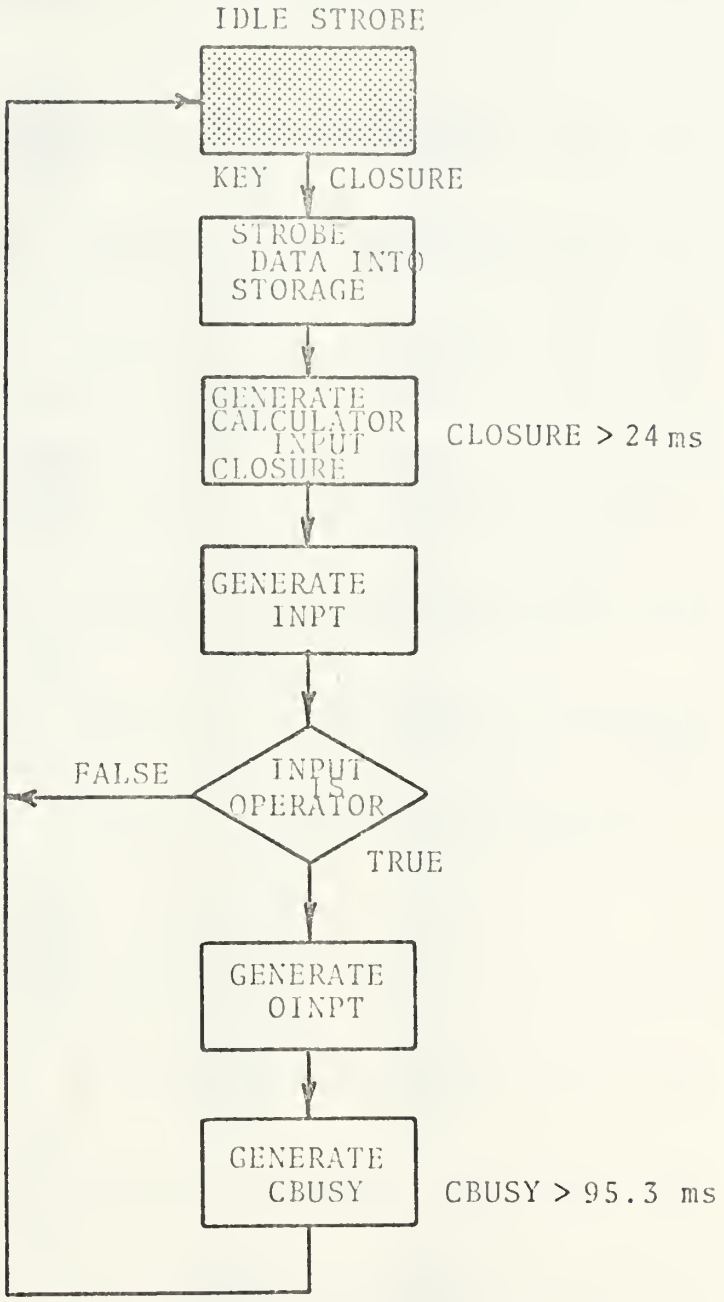


FIGURE 12 SEQUENCE OF OPERATIONS FOR THE INPUT SECTION

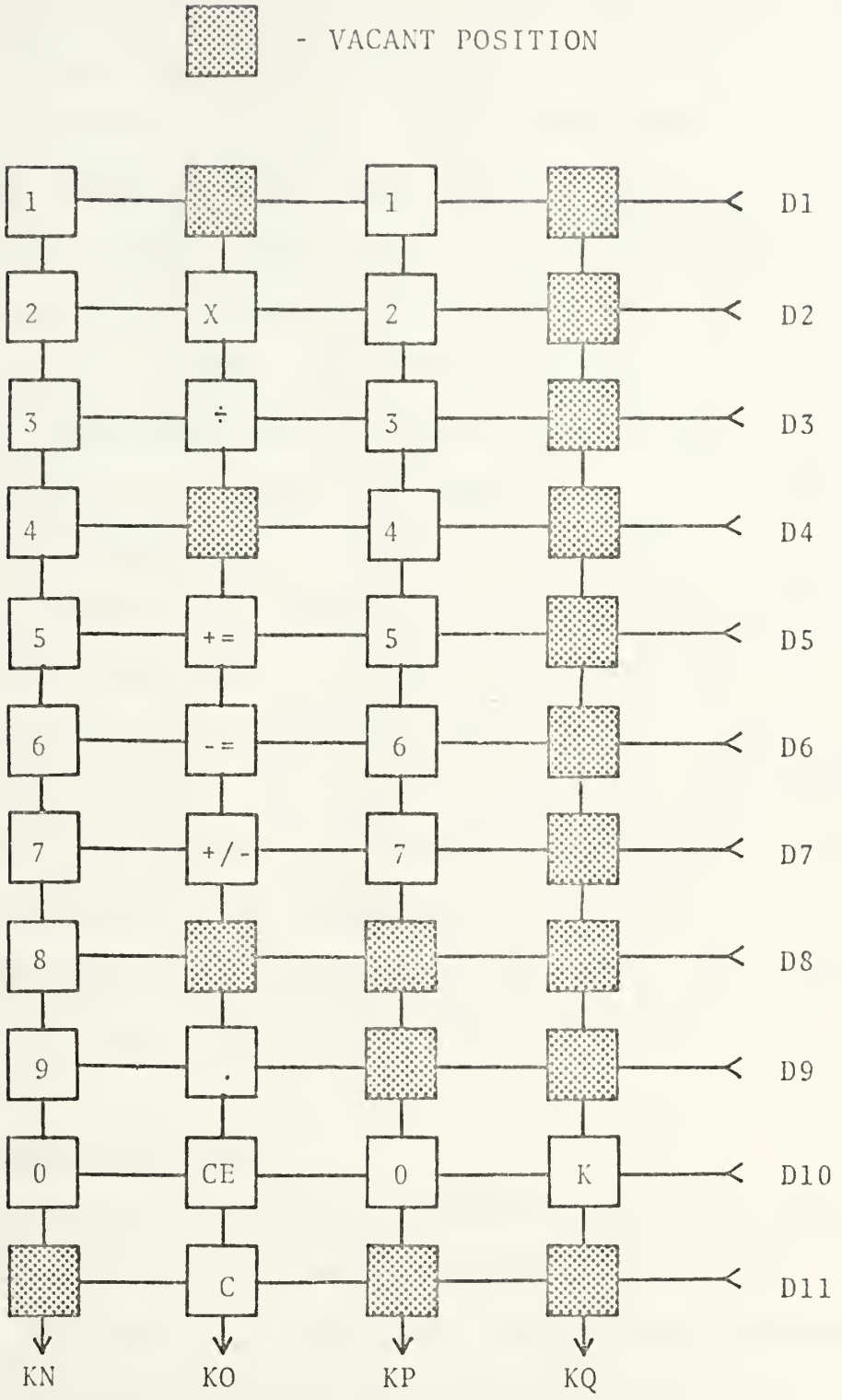


FIGURE 13 CALCULATOR KEYSWITCH MATRIX

loading on the interface circuits. The scheme used to provide both the matrix configuration and the TTL-MOS interface is shown in figures 14 and 15. Type 7426N gates are 2-input NAND's with a high-voltage, open-collector output structure. Pull-up of both input lines to Vss is provided by a 1kΩ resistor. The digit drive lines are fed back from the output interface and are sequentially scanned as previously described. The input control lines are low-active; therefore, if there are no inputs, the input line will be held at logical 0 sequentially, in turn, by the 7426N gates. If an input is present, that particular line will be low for a period greater than 20ms. Then the input line will be pulled up to logical 1 during the time frame indicated by the digit drive line to that particular gate. This results in the same input sequence as a standard keyswitch at that point in the matrix. The arrangements used for both the numeric and operational input lines are shown. The keyboard point (KP) and keyboard constant (KQ) lines will be discussed later.

2. Output Interface

The output interface is a MOS-TTL interface and poses a different problem. The loading conditions that must exist are shown in figure 16. The output lines of the MOS calculator are open-drain buffers and utilize the same positive logic scheme as the input. An active output or one that is at logical 1 is in conduction at Vss (+7.5V) with a typical source impedance of 250Ω. Since for a logical 1 input the

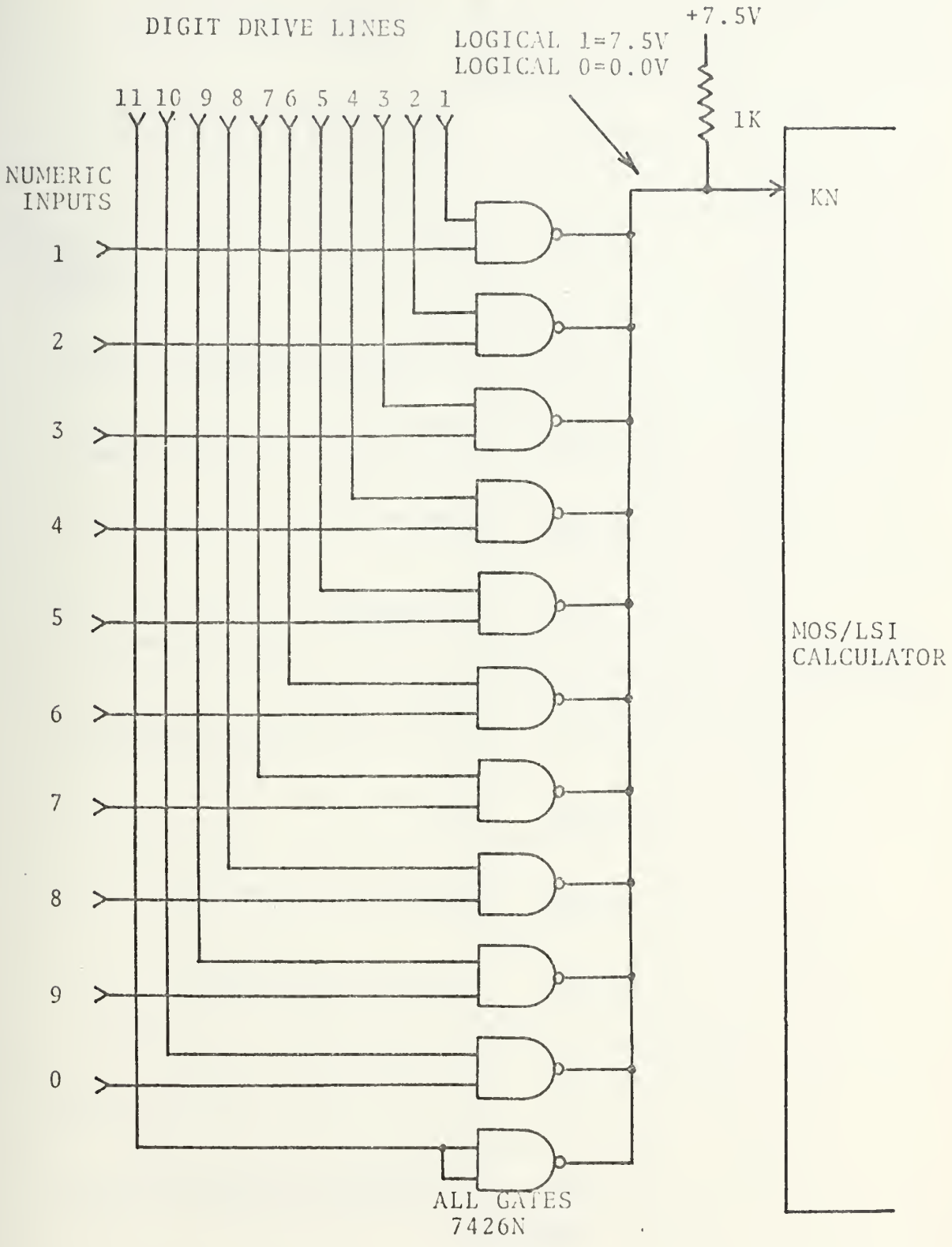


FIGURE 14 TTL-MOS INTERFACE FOR NUMERIC INPUT LINE

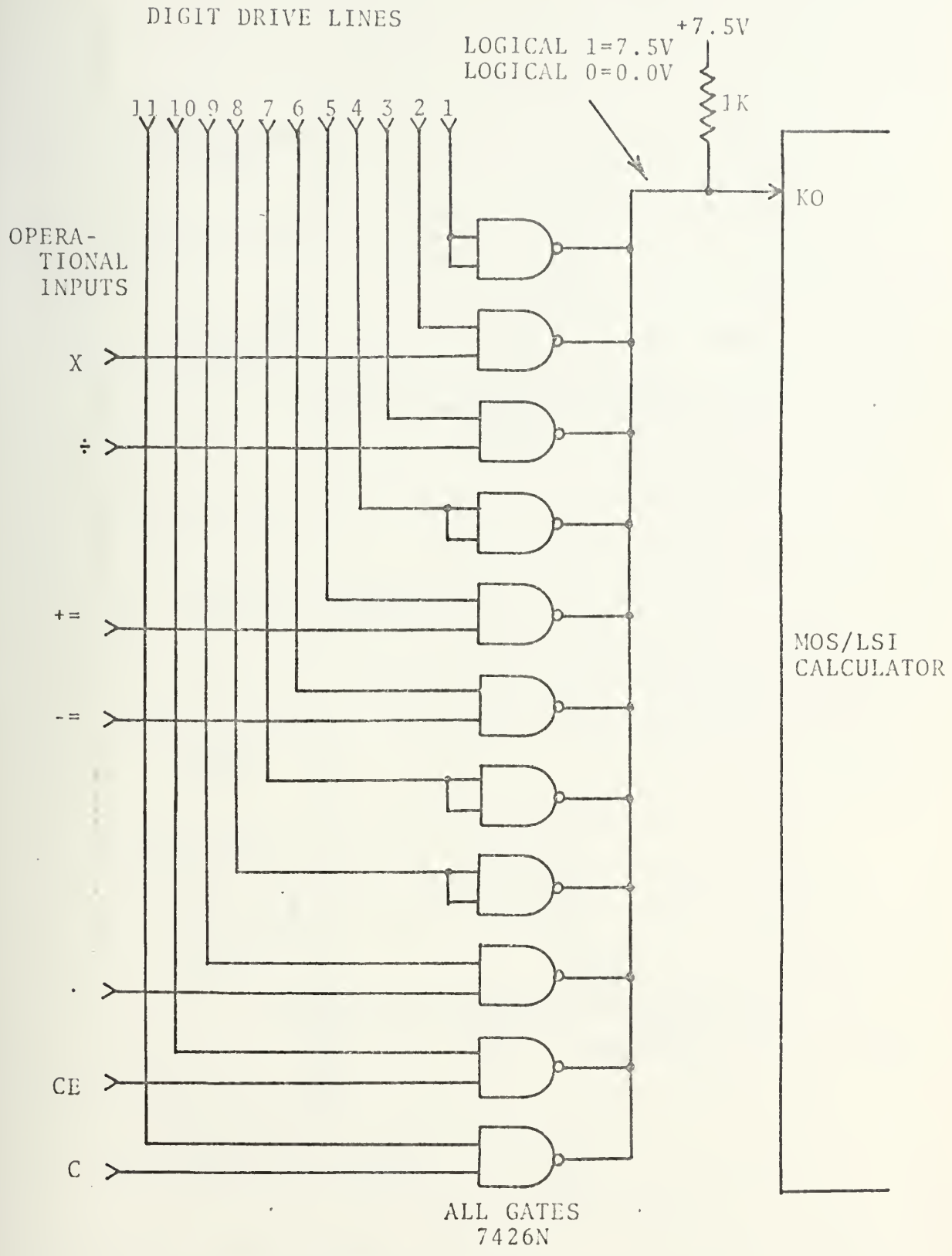
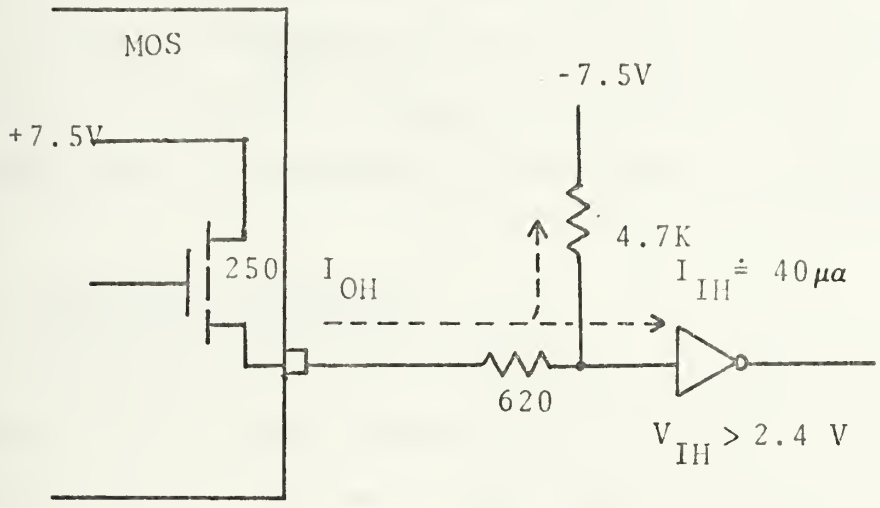
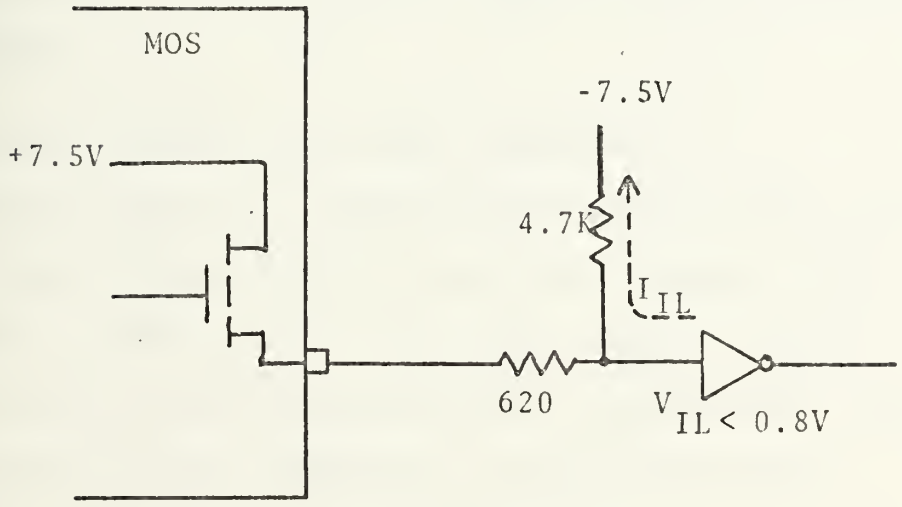


FIGURE 15 TTL-MOS INTERFACE FOR OPERATIONAL INPUT LINE



a. LOGICAL 1 OUTPUT



b. LOGICAL 0 OUTPUT

FIGURE 16 OUTPUT MOS-TTL INTERFACE LOADING CONDITIONS

TTL gate require only approximately 40 μA, the requirement is one of level shifting with the condition of Vih > 2.4 V. For the logical 0 case, the output buffer is essentially open. The input loading on the TTL gate, in this case, is typically 1.6 mA with a voltage requirement of Vil < 0.8 V. Both conditions of interface are met with the structure shown.

3. Additional Features

The remainder of the calculator circuitry is shown in figure 17. A clock frequency of 307 kHz with appropriate level shifting is provided. Power supply voltages are derived from a simple zener diode regulator circuit. The constant mode of operation and selectable fixed decimal positions are provided by jumper connections at the appropriate points in the matrix. These could be replaced by switches.

D. CODE CONVERSION AND DATA PROCESSING

Code conversion to BCD format for the format section and output multiplexer is done after the MOS levels are shifted to TTL levels. The seven-segment information and digit drive line D11 are used for this purpose. Sign, error and leading zero information are made available.

1. Seven-Segment to BCD Converter

The converter is a combinational circuit and is shown as the upper portion of figure 18. Initial design of the circuit was done using a Karnaugh map. This design was

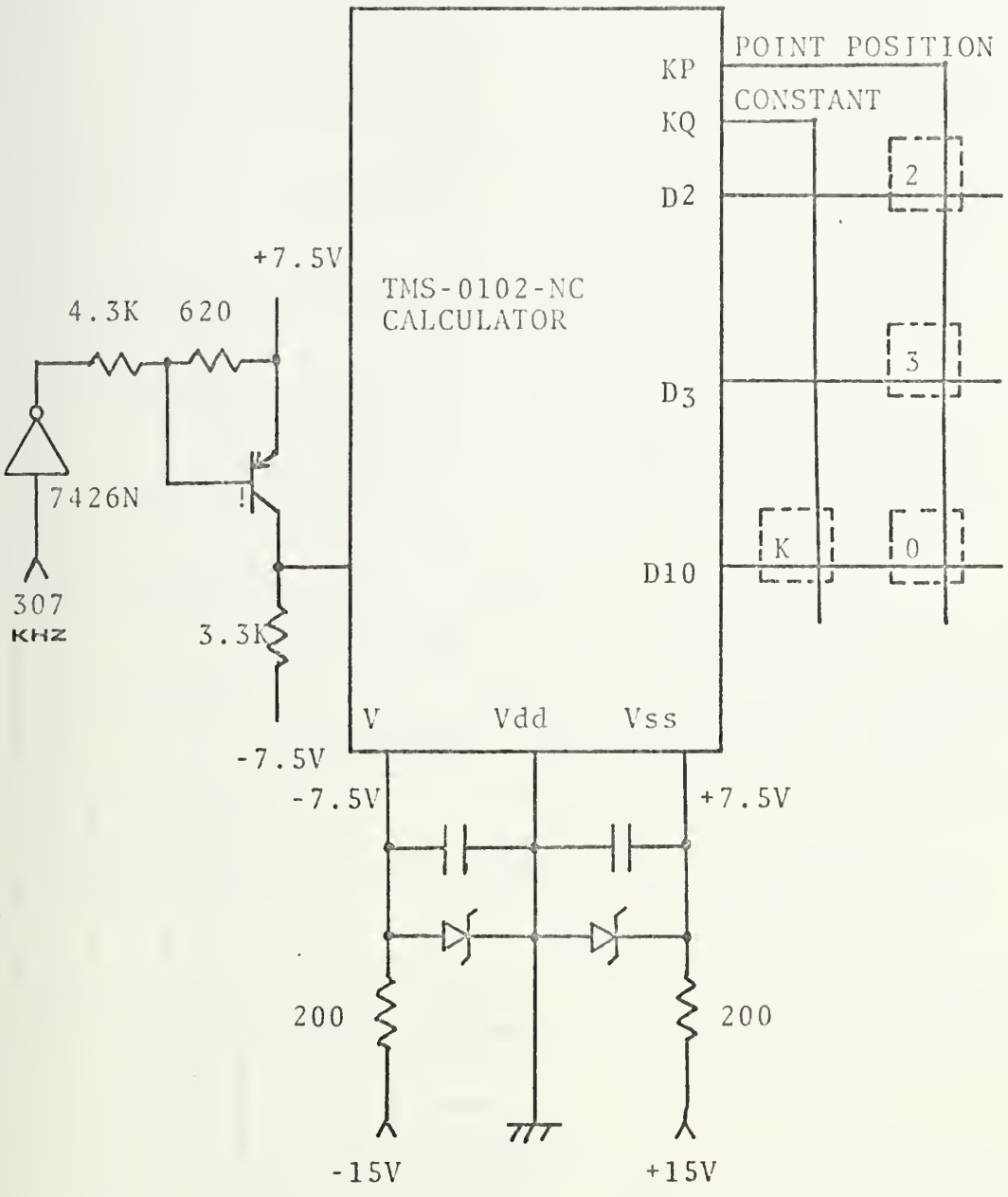


FIGURE 17 ADDITIONAL CALCULATOR CIRCUITRY

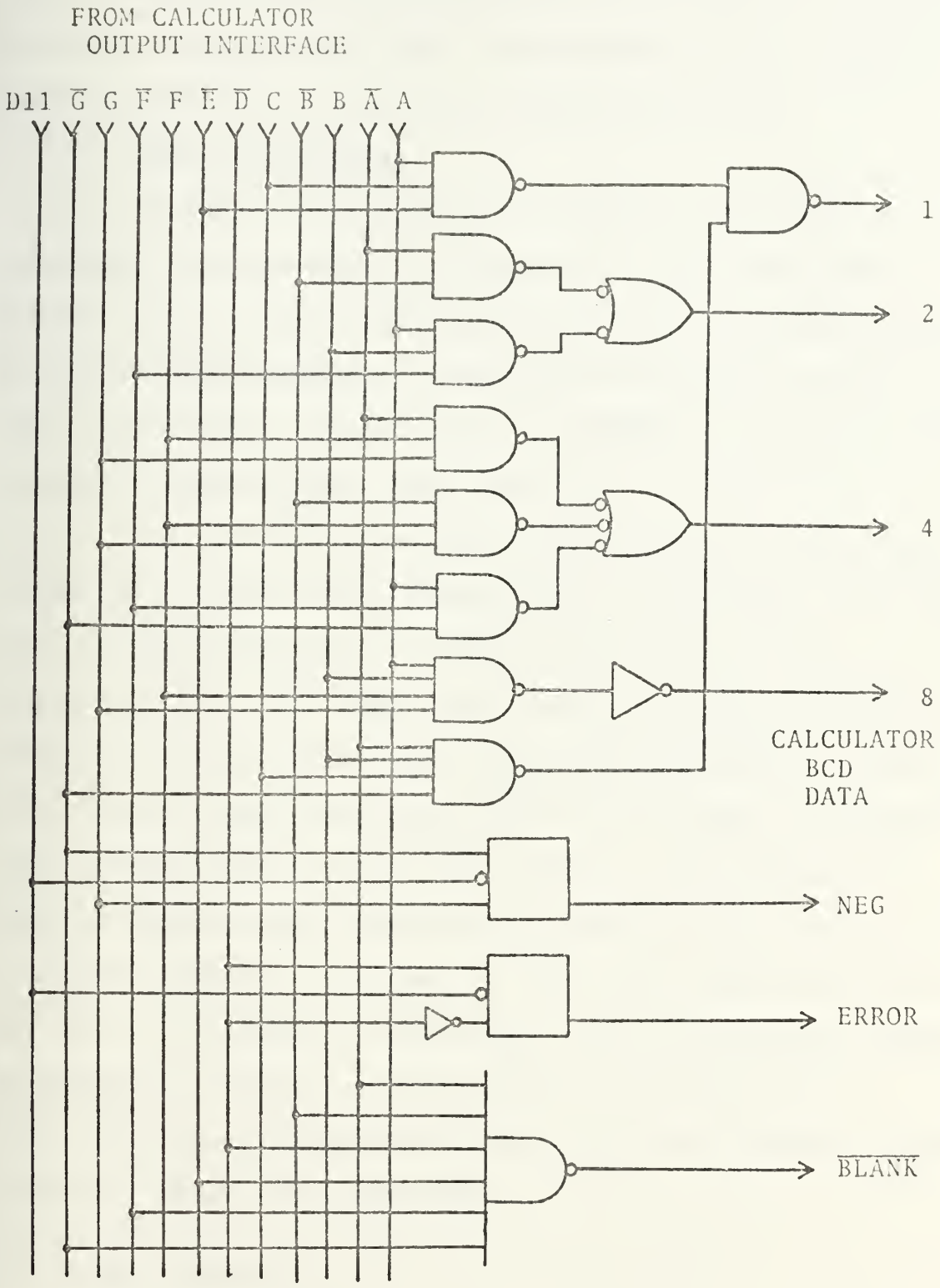


FIGURE 18 CODE CONVERSION AND DATA PROCESSING

later verified using the Quine-McCluskey reduction techniques discussed in reference [11]. The BCD data at the output is then transmitted to the output data multiplexer.

2. Other Indications

Leading zero blanking is provided by detecting the condition of all segments at logical 0. The calculator detects leading zeros internally and uses this method to produce a blanked position in the time multiplexed display. The presnece of a blanked position, $\overline{\text{BLANK}}$, is passed to the output data multiplexer for later use.

The calculator presents sign and error conditions by outputing certain seven-segment codes during digit time frame D11. A negative result is indicated by the presence of segment G only. The four error conditions of positive and negative result overflow are indicated by presence of segment D and others during this digit time frame. Therefore, this information is extracted as shown. If segment G is present during digit time D11, the flip-flop is cleared and a logical 1 at NEG is passed to the output data multiplexer for use. If segment D is present, the same sequence results in ERROR at logical 1. The state of the flip-flops is reversed within one display cycle time of the actual change of status within the calculator.

E. FORMAT SECTION

The format generation section is the single most important section in the 4010 calculator option. This circuit

provides the timing control necessary to generate the desired terminal display screen format. The actual circuit detail is too complex to be presented within this document but are available in the complete circuit blueprints. Instead, a simplified block diagram is presented as figure 19. The primary control levels are the phase control lines from the phase decoder. Additional control levels are received from the calculator input and output sections, and from the terminal buss structure.

During all phases except phase 1 a strobe timing signal, CSTRB, is generated for the strobe generation circuit, which is to be discussed later. An interrupt on this timing signal is generated if either $\overline{\text{TBUSY}}$ or $\overline{\text{CBUSY}}$ is present. CSTRB is generated by two means. One is an automatic strobe at a rate determined by a frequency division down from 307 kHz. This was set to be less than the maximum character processing rate of the 4010 terminal. The second source of CSTRB is from the phase 6 timing circuitry.

1. Phase 1

During phase 1, data transmission from the calculator is at a rate determined by the keyboard in use. During this phase, the format circuitry gates the signal INPT, received from the calculator input section, to the counter COUNTI, and thus counts the number of keyboard inputs. This action continues until an operational input, OINPT, is received. OINPT is one of the several signals that provide a clocking of the phase counter to the next phase. During phase 1,

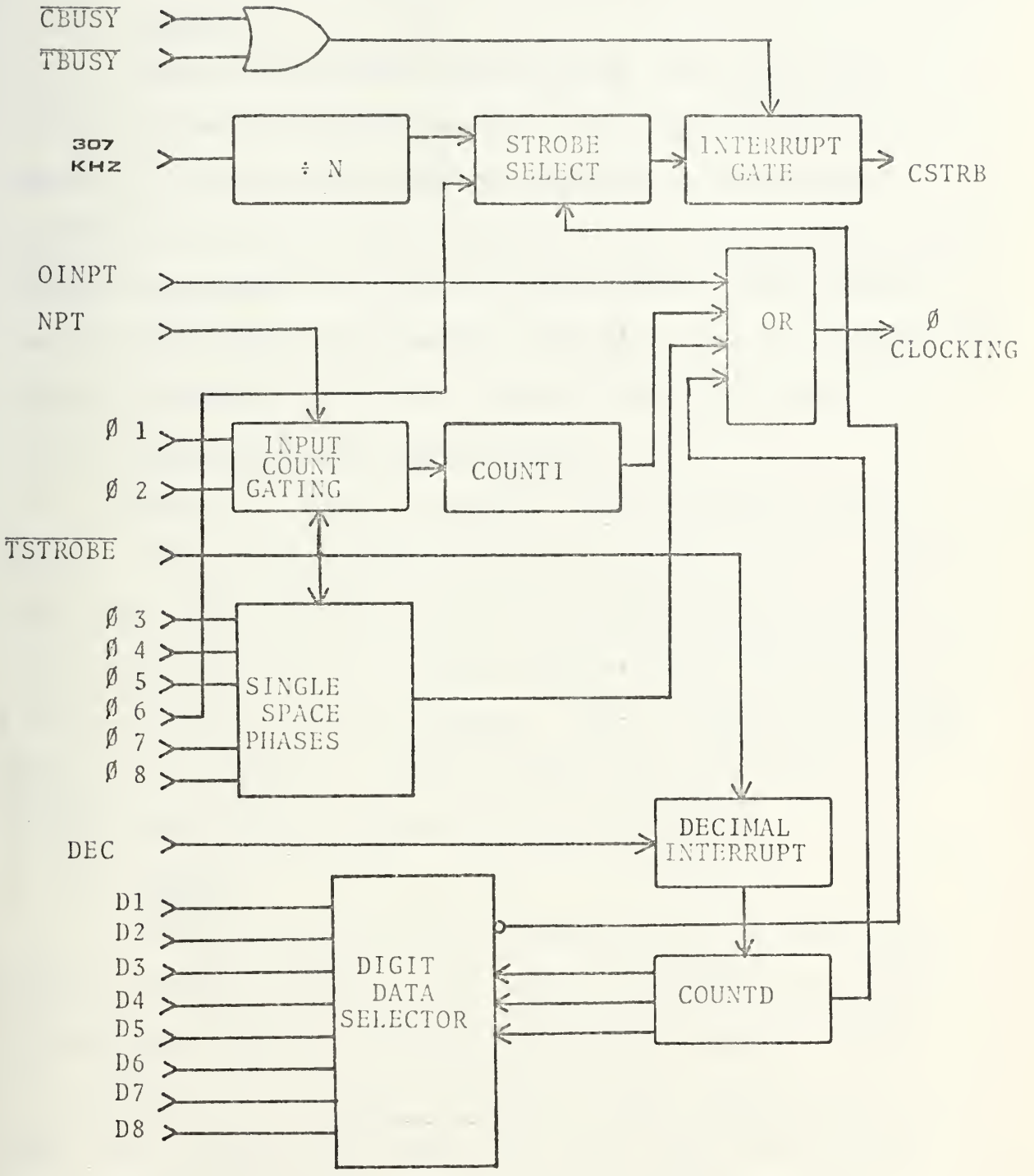


FIGURE 19 FORMAT SECTION BLOCK DIAGRAM

CSTRB is generated at the automatic rate but is ignored by the strobe generation circuit.

2. Phase 2

Reception of OINPT during phase clocks the phase counter to the next state and puts the format circuit into phase 2. In this phase CSTRB is provided to the strobe generation circuits at the automatic rate, and the resultant $\overline{\text{TSTROBE}}$ generated are gated to clock COUNTI. When COUNTI reaches count 16, a combination circuit at its output provides a phase clocking signal which shifts control to phase 3.

3. Single Character-Space Phases

Phases 3-5 and 7-8 are all single character-space phases. The action within the format circuit is the same in each case. The presence of an active state on any one of these phase control lines allow exactly one strobe generation before clocking to the next phase. This is done by allowing CSTRB to be generated at the automatic but using the first $\overline{\text{TSTROBE}}$ generated to provide the phase clocking.

4. Phase 6

During phase 6 data is transmitted at a rate determined by several factors. The source of CSTRB is switched to the digit strobe. Initially the digit counter, COUNTD, is in state 0. This stage in binary form is used by the digit data selector to select the digit drive line of the most significant digit. This results in generation of CSTRB at the same instant that the particular data line selected is active. Since both the calculator BCD data at

the output data multiplexer and the selected digit drive line are active for a longer period of time required to enter the character into the terminal, the correct digit information is displayed. The $\overline{\text{TSTROBE}}$ generated for this purpose also clocks COUNTD to select the next most significant digit, and the process is repeated. If the decimal point is detected during a given digit time frame a one-character space interrupt is generated, during which time the decimal point is transmitted to the terminal. When the counter reaches its eighth state,it provides a phase clocking to shift control to the next phase.

F. OUTPUT DATA MULTIPLEXER

The output data multiplexer operates in close conjunction with the format generation section. Whereas the format section ensures the line format by controlling the strobe generation process, the output data multiplexer ensures that the correct codes are put onto the data busses. A block diagram of the multiplexer is shown as figure 20. Again the primary control lines are the phase lines from the phase counter. These lines determine which data inputs are selected for transmission. The data selection is done by six type 74151N 1-1N-8 data selectors.

During Phase 1, the keyboard bits are selected. During phase 2, hardwired SP code inputs are selected. During phase 3, a NUL code is selected if error is not present, and a BEL code if error is present. During phase 4, a SP

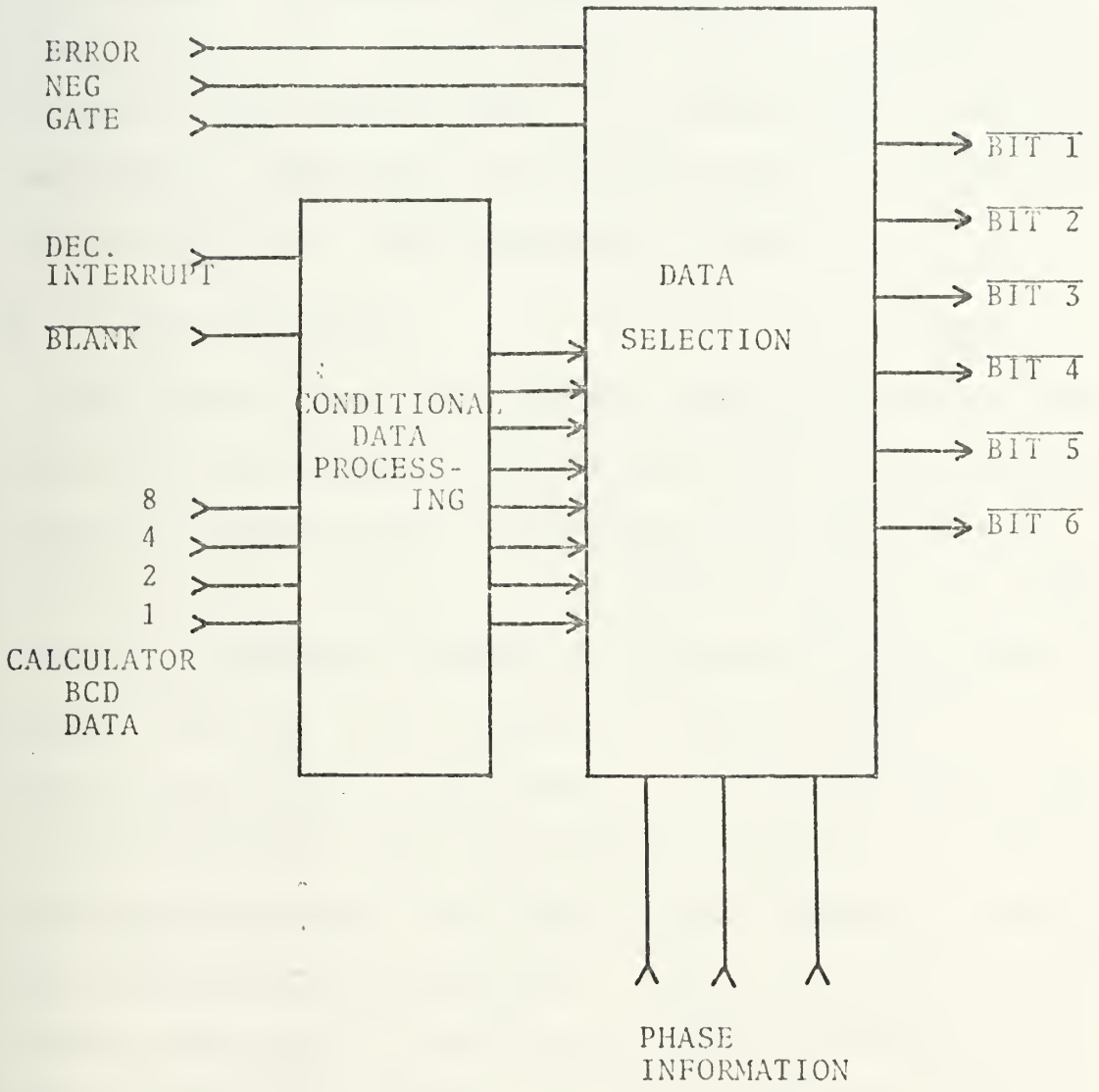


FIGURE 20 BLOCK DIAGRAM OF OUTPUT DATA MULTIPLEXER

code is selected if error is not present, and a # code if error is present. Phase 5 results in the selection of a - code if NEG is active, and a SP if not. During phase 6 the BCD calculator data is selected provided neither $\overline{\text{BLANK}}$ or decimal interrupt is active. If BLANK is active, a SP code is selected. If decimal interrupt is active a decimal point code is selected. Phases 7 and 8 result in selection of a CR and LF codes respectively. In each case the data bits selected are gated onto the terminal busses by a data gate received from the strobe generator circuit.

G. STROBE GENERATOR

The strobe generator receives timing information from the format and keyboard circuits and generates the strobe sequence discussed under preliminary considerations in section II-B-1. The circuit is shown in figure 21. When enabled, $\overline{\text{TSTROBE}}$ and $\overline{\text{CSTROBE}}$ are generated upon command by signals from one of two sources. During phase 1, a keyboard circuit exactly the same as the one utilized by the terminal generates both the keyboard data bits for the output data multiplexer and the timing signal KSTROBE to initiate the strobe generation sequence. During all other phases, strobe generation is initiated by CSTRB received from the format generation circuit. In addition to the strobe signals, a data gate is provided for the output data multiplexer.

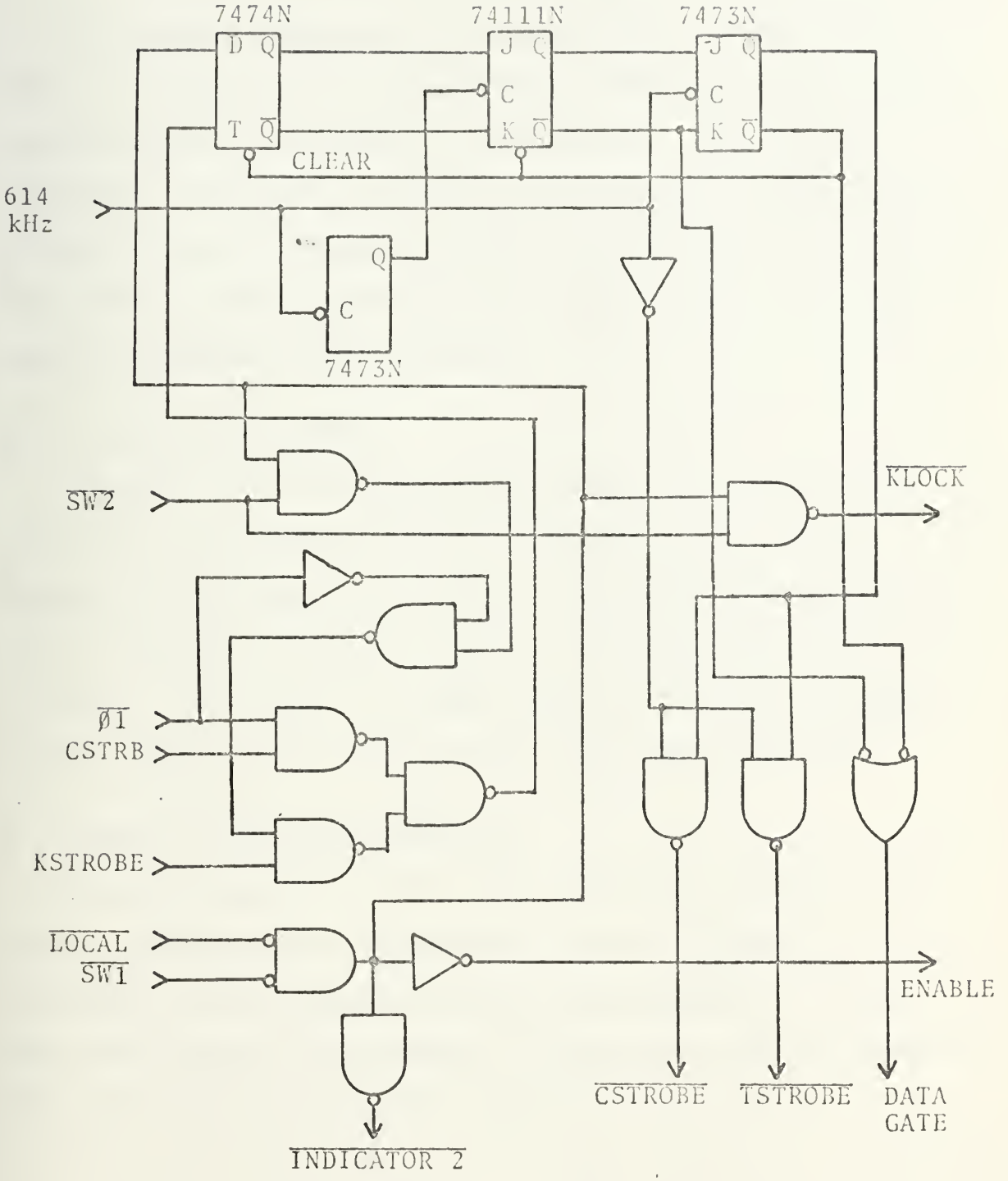


FIGURE 21 STROBE GENERATION CIRCUIT

IV. RESULTS

Preliminary debugging of the calculator option prototype was accomplished in three days. Only one major problem was discovered subsequent to this period. This was the result of a design error in the seven-segment to BCD code conversion in the calculator output section, and resulted the number 4 being decoded as a 5. The circuit was redesigned and the problem corrected.

A. CALCULATION EXAMPLES

Appendix A is a collection of examples of actual calculations performed using the calculator option. The examples were chosen to illustrate both the versatility of the TMS-0102NC calculator, and the resultant screen format obtained. The copies were made directly from the terminal display screen using the Tektronix 4601 Hard Copy Unit.

B. OVERALL CALCULATOR OPERATION

Overall operation of the 4010 calculator option, and a general description of the display action obtained is contained in the document presented as Appendix B. This paper was written for Tektronix to provide a general description of the operation of the circuit.

V. CONCLUSIONS AND RECOMMENDATIONS

From the standpoint of operation, the design of the calculator option and resultant proper operation are considered a success. However, the large amount of complex circuitry involved in interfacing a calculator intended for simple desktop machines with the 4010 terminal and producing the desired screen format of the result increases the cost to the point where production of the calculator option is questionable. Certainly improvements could be made with no reduction in capability by using a calculator with a BCD coded form of output, thereby eliminating some of the data processing circuitry; but the resultant reduction in cost does not justify additional work. Therefore, further investigation in the present form of the calculator is not recommended. Instead, a new approach to the "hardwired" form of terminal intelligence is proposed.

In recent years, complete general purpose computers have become available completely contained on a few MOS/LSI integrated circuits. These microcomputers, presently available from several companies, are designed with dedicated, special-purpose applications in mind where small size and low cost are desirable. The uses of microcomputers are many. Present sets are being utilized in production systems ranging from point-of-sales terminals to electronically controlled household ranges. In addition, the microcomputers

can be programmed to function as scientific calculators. These functions would be particularly desirable to almost every user of present day computer display terminals. In addition, all of the format generation accomplished in the present version by complex sequential and combinational circuits could be done within the microcomputer through use of microprogramming. This would reduce the option configuration to the microcomputer set itself, and a simple interface.

An initial, general investigation into microcomputers was performed as a project for EE-4823, Advanced Digital Computer Systems. This study resulted in the selection of the SK-0030 version of National Semiconductors Microprogrammable Arithmetic Processor (MAPS) as particularly worthy of further investigation. In fact, this set was identified early in the project as one of the most attractive possibilities, but the devices were not available early enough for the project.

APPENDIX A: CALCULATION EXAMPLES

EXAMPLE: ADDITION/SUBTRACTION

MODE: CHAIN

POINT: 2

		0
12+		12.00
12+		24.00
12+		36.00
369+		405.00
456+		861.00
1000-	-	139.00
123+	-	16.00
123+		107.00
789+		896.00
12.36+		908.36
36.56+		944.92
4563+		5507.92
2+		5509.92
9213-	-	3703.08
4000+		296.92

POINT: 3

1+		297.920
1+		298.920
123+		421.920
300-		121.920
200+		321.920
258-		63.920
300-	-	236.080
123-	-	359.080
500+		140.920
123+		263.920

POINT: FLOATING

		0
1+		1
1+		2
2+		4
369+		373
23.36'+		396.36
45.36+		441.72
456+		897.72
1000-	-	102.28
256+		153.72
369+		522.72
365+		887.72
456.36+		1344.08
1236.54+		2580.62
3000-	-	419.38
456+		36.62
36.62-		0
200+		200
200+		400
200+		600
200+		800
1000-	-	200
1236+		1036
333333+		334369
333333+		667702
333333+		1001035
45632+		1046667
456+		1047123
1+		1047124
20000+-		1027124

EXAMPLE: CHAIN CALCULATIONS

MODE: CHAIN

POINT: FLOATING

	0
2+	2
23+	25
256+	281
/	281
2+	140.5
/	140.5
99+	1.4191919
*	1.4191919
36+	51.090908
*	51.090908
36+	1839.2726
*	1839.2726
2+	3678.5452
*	3678.5452
6+	22071.271
*	22071.271
6+	132427.62
*	132427.62
6/	794565.72
9*	88285.08
23/	3838556.8
99+	38510.674
	0
2*	2
2*	4
2*	8
2*	16
2*	32
2*	64
2*	128
2*	256
2*	512
/	512
56+	9.1428571
/	9.1428571
79+	1.015873
/	1.015873
66+	0.015392
*	0.015392
66/	1.015872
1+	1.015872
	0
123+	123
654+	777
789+	1566
*	1566
3/	4698
2*	2349
65/	152685
9+	16865
/	16865
999+	16.981981
*	16.981981
65+	1102.8287
*	1102.8287
65+	71748.865
*	71748.865
369+	26475331
/	26475331
69+	383700.44
/	383700.44
36*	10658.345
6+	63950.07

EXAMPLE: SQUARES

MODE: CHAIN

POINT: FLOATING

```
                    0
2*                  2
+                   4
12*                12
+                 144
25*                25
+                 625
456*              456
+              207936
1452*            1452
+           2108304
```

POINT: 2

```
2*                  2
+                4.00
12*                12
+              144.00
456*              456
+           207936.00
789*              789
+           622521.00
9*                  9
+               81.00
7*                  7
+               49.00
6*                  6
+               36.00
9*                  9
+               81.00
36*                36
+             1296.00
22*                22
+              484.00
99*                99
+             9801.00
```

POINT: 3

```
                    0
1*                  1
+               1.000
8*                  8
+              64.000
369*             369
+          136161.00
5*                  5
+              25.000
78*                78
+            6084.000
6*                  6
+              36.000
```

EXAMPLE: CONSTANT DIVISION

MODE: CONSTANT

POINT: FLOATING

456/	456
2+	228
4+	2
5+	2.5
6+	3
69+	34.5
456.321+	228.1605
12+	6
365+	182.5
78+	39
456+	228
589.32+	294.66

POINT: 2

	0
78/	78
2+	39.00
123+	61.50
45+	22.50
36+	18.00
236+	118.00
123+	61.50
123.369+	61.68
78.96+	39.48
45.36+	22.68
45.23+	22.62
5+	2.50
6+	3.00

POINT: 3

	0
8/	8
3+	2.667
456+	152.000
36+	12.000
23+	7.667
235+	78.333
5796+	198.667
45+	15.000
3+	1.000
36+	12.000
9+	3.000
8+	2.667
35+	1.667
74+	24.667
45+	15.000
36+	12.000
98+	32.667

EXAMPLE: CONSTANT MULTIPLICATION

MODE: CONSTANT

POINT: 3

```
                          0
.05*                   0.05 POINT: FLOATING
100+                  5.000
123+                  6.150 /                      12.00
23.36+                1.168                           0
456.23+              22.812 2.36*                   2.36
45+                   2.250 2+                      4.72
36.55+                1.828 3+                      7.08
789+                 39.450 36+                    84.96
123.56+               6.178 56+                   132.16
1000+                50.000 36.35+                85.786
78.9955+              3.950 456.23+          1076.7028
123+                  6.150 23.56+             55.6016
3654+               182.700 36+                   84.96
256+                 12.800 789.36+          1862.8896
```

POINT: 2

```
                          0
2*                        2
56+                   112.00
36+                    72.00
23+                    46.00
2.36+                   4.72
78.369+               156.74
5+                     10.00
2+                      4.00
3+                      6.00
6+                     12.00
```

```
EXAMPLE: POWERS

MODE: CONSTANT

POINT: FLOATING
```

```
                        0
2%                      2
+                       4
+                       8
+                      16
+                      32
+                      64
+                     128
+                     256
+                     512
+                    1024
+                    2048
+                    4096
+                    8192
+                   16384
+                   32768
+                   65536
+                  131072
+                  262144
+                  524288
+                 1048576
+                 2097152
+                 4194304
+                 8388608
+                16777216
+                33554432
+                67108864
+             # 1.3421772
+             # 1.3421772
```

```
                        0
3%                      3
+                       9
+                      27
+                      81
+                     243
+                     729
+                    2187
+                    6561
+                   19683
+                   59049
+                  177147
+                  531441
+                 1594323
+                 4782969
+                14348907
+                43046721
+             # 1.2914016
                        0
                     2.99
+                    8.9401
+                   26.730899
+                   79.925388
+                   238.97691
+                   714.54096
+                   2136.4774
+                   6388.0674
+                   19100.321
+                   57109.959
+                   170758.77
+                   510568.72
+                   1526600.4
+                   4564535.1
+                   13647959
+                   40817297
+             # 1.2201411
+             # 1.2201411
```

EXAMPLE: OVERFLOW INDICATION

MODE: CHAIN

POINT: FLOATING

```
                              0
9*                            9
9*                           81
9*                          729
9999*                   7289271
99*                  # 7.2163782
```

EXAMPLE: INPUT ERROR INDICATION

MODE: CHAIN

POINT: FLOATING

```
                              0
12.369+                  12.369
23+                      35.369
36.55+                   71.919
111+                    182.519
123456789+          # 12345868
```

EXAMPLE: UNDERFLOW INDICATION

MODE: CHAIN

POINT: FLOATING

```
                              0
9/                            9
9/                            1
9/                    0.1111111
9/                    0.0123456
9/                    0.0013717
9/                    0.0001524
9/                    0.0000169
9/                    0.0000018
9/                    0.0000002
79./                            0
9/                              0
```

APPENDIX B

TEKTRONIX 4010
COMPUTER DISPLAY TERMINAL
CALCULATOR OPTION

Bill Cherry - September 18, 1972

1. GENERAL DESCRIPTION

The 4010 calculator option is a terminal auxiliary card, which, when installed in the 4010 terminal, provides the user with an eight-digit, five function calculator. The functions of addition, subtraction, multiplication, and division are obtained through a single key-stroke with both the entry and results displayed sequentially on the 4010 screen. A fifth function, that of the square of a number, can be obtained through a two key-stroke sequence. Data input to the calculator is either through the calculator keyboard, provided on a cable extention from the calculator board, or through the terminal keyboard. The format of the calculator is that of a business calculator with the functions of addition and subtraction resulting in an accumulation type operation.

2. CAPABILITIES

A. Range of Operation

Number of digits displayed is eight. Answers greater than 99999999 result in overflow. Overflow is one of the several error conditions that sound the terminal bell and print the # by that result to indicate to the operator that an error has been made. Answers less than 0.0000001 result in underflow. Underflow condition is indicated by a single 0 in the results column. Both overflow and underflow conditions prevent further calculations until the calculator is cleared by depressing the clear (C) key.

Numeric input of greater than eight digits results in an error condition and error indications as described previously.

B. Operations

Operation	Key	ASCII
Addition	+ =	+
Subtraction	- =	-
Multiplication	X	*
Division	÷	/
Square	X,+=	* , +

Operation of the clear (C) key clears all of the calculator registers. This action is verified by the printing of a single 0 in the results column. Operation of the clear-entry (CE) key clears the input register only. Previous results as stored in the accumulator register are saved.

A page key is provided on the calculator keyboard for the convenience of the user. The terminal screen can be erased without clearing the calculator.

C. Decimal Point

Both fixed-point and floating-point conditions are possible. The type of operation, and the point position in the fixed point case, is switch selectable.

Switch	DECIMAL POINT
F	FLOATING
0	POSITION 0
2	POSITION 2
3	POSITION 3

In the fixed point mode, all answers are automatically rounded off (4/5 round-off) to the position selected.

Example: Answer = 1.23781
Point Position = 2

Display 1.24

Leading zeros are suppressed in both point modes. Trailing zeros are suppressed in the floating point mode only. If the result exceeds the space available for a given fixed point mode, the calculator protects the most significant digits by automatically shifting the point right.

D. Mode of Operation

Mode of operation, chain or constant, is selected using the K switch. With the K switch off, normal chain-type operations result. With the K switch on, constant type operations are possible in multiplication and division.

Multiplication: The constant multiplier is the first numeric input. This is followed by the multiplication (X) key. Then any number can be multiplied by the constant by simply entering the number and then depressing the + = key. The number input is displayed in the left (input) column while the answer is displayed in the right (results) column.

Division: Operation is as above only with the division key utilized second. The constant divisor is also the second numeric entry, vice the first as in multiplication. (See example calculations).

An additional feature of the constant mode of operation is that once a constant multiplier or divisor is set up in the calculator, repeated depresssions of the + = key without numeric inputs results in the previous result multiplied or divided by the constant. This enables the operator to find sequential powers of a given number very quickly.

3. OPERATION

The calculator mode of operation is enabled by switching the terminal to local and turning switch 1 on. Switch 2 is used to select the keyboard to be used.

Addition: Enter number to be added, then depress = + key.

Subtraction: Enter number to be subtracted, then depress - = key.

Multiplication: Enter first number, then depress X key. The first input is verified in the results column. Enter the second number, then depress the + = key. The answer is obtained in the results column.

Division: Enter the number to be divided, then depress ÷ key. First number is verified in the results column. Enter the divisor, then depress the = = key. The answer is obtained in the results column.

Square: Enter the number to be squared, then depress the X key. The number is verified in the results column. Next depress the + = key to obtain the square directly below the number in the results column.

LIST OF REFERENCES

1. Tektronix Inc., 4010 and 4010-1 Users Manual, 1972.

2. Tektronix Inc., Engineering Instrument Specification-4010 and 4010-1 Computer Display Terminals, 1972.

3. Tektronix, Inc., Designing Parallel Interfaces for the 4010 Terminal, 1971.

4. Peatman, J. B., The Design of Digital Systems, McGraw-Hill, 1972.

5. Texas Instruments Inc., The Integrated Circuits Catalog for Design Engineers, 1972.

6. Texas Instruments Inc., Designing with TTL Integrated Circuits, 1971.

7. Fitchen, F. C., Electronic Integrated Circuits and Systems, Van Nostrand Reinhold, 1970.

8. Texas Instruments Inc., MOS/LSI Design and Application, 1972.

9. Givone, D. D., Introduction to Switching Circuit Theory, McGraw-Hill, 1970.

10. Burroughs Corporation, Digital Computer Principles, 1961.

11. McCluskey, E. J., Introduction to the Theory of Switching Circuits, McGraw-Hill, 1965.

12. Texas Instruments Inc., TMS-0100NC MOS/LSI One-Chip Calculator Series For Design Engineers, 1973.

13. Bell and Newell, Computer Structures, McGraw-Hill, 1971.

14. Banjerji, R. B., Theory of Problem Solving, American Elsevier, 1969.

15. Slagle, James R., Artificial Intelligence: The Heuristic Programming Approach, McGraw-Hill, 1969.

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ABSTRACT

Recent advances in Metal-Oxide-Semiconductor/Large-Scale-Integration (MOS/LSI) circuits have made large amounts of computational capability available in small packages. One such MOS/LSI circuit, a business-format, four-function calculator, is utilized to provide a fixed-function form of intelligence in the Tektronix 4010 Computer Display Terminal. Discussion of important circuit design concepts from preliminary considerations to final testing and results is presented. Sample calculations and instructions for calculator operation are given as appendices.

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	ROLE	WT	ROLE	WT	ROLE	WT
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Computer Terminal						

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C4154 Cherry
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